CH643 Datasheet

V1.2

http://wch-ic.com

Overview

CH643 is an industrial-grade RGB display driver microcontroller based on the QingKe RISC-V core. CH643 has built-in USB and PD PHY, supports USB Host and USB Device function, USB PD and type C fast charging function, PWM drive RGB LED function, built-in programmable protocol I/O controller, provides 2 sets of OPA, 3 sets of CMP voltage comparators, 4 sets of USART serial ports, I2C, SPI, multiple timers, 12-bit ADC, 15-channel Touchkey and other rich peripheral resources.

Features

- **Core**
  - QingKe 32-bit RISC-V4C core
  - Support RV32IMAC instruction set and self-extending instructions
  - Fast programmable interrupt controller + hardware interrupt stack
  - Branch prediction, conflict handling mechanism
  - Single-cycle multiplication, hardware division
- **Memory**
  - 20KB volatile data storage area SRAM
  - 62KB program memory area CodeFlash
  - 3328B system boot program memory area BootLoader
  - 256B system non-volatile configuration information memory area
  - 256B user-defined information storage area
- **Power management and low power:**
  - System power supply V_{DD} rated voltage: 3.3V or 5V
  - Low power modes: Sleep, Stop, Standby
- **Clock & Reset**
  - Built-in 48MHz RC oscillator
  - Power on/down reset, programmable voltage detector
- **8-channel general-purpose DMA controller**
  - 8 channels, support ring buffer management
  - Support TIMx/ADC/USART/I2C/SPI
- **Programmable Protocol I/O Controller PIOC:**
  - Programmable, supports a wide range of 1-wire interfaces, 2-wire interfaces
- **2-group OPA/PGA/voltage comparator:**
  - Multiple input channels, selectable multi-step gain
  - 2 output channels each, optional ADC pins
- **3-group analog voltage comparator CMP:**
  - 2 input channels each, optional common reference voltage pin
  - Output to I/O or internal direct trigger TIM2
- **RGB tri-colour LED pulse width modulation LEDPWM:**
  - Built-in 3*16=48 channel PWM current drive, support COM scan
  - Fully built-in support for 192 RGB or 576 monochrome LEDs
  - External PMOS supports 288 RGB groups or 864 monochrome LEDs
  - 24-bit colour data, up to 16777216 colour combinations
  - 8-bit luminance data, up to 256 levels of grey scale
  - Support Matrix keyboard scanning
- **12-bit ADC**
  - Analogue input range: GND ~ V_{DDA}
  - 15-channel external signal + 1-channel internal signal channel
- **15-channel Touch-Key detection Timers**
- **Multiple timers**
  - 2×16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 1×16-bit general-purpose timers, provide input capture/output comparison/PWM
  - 2 watchdog timers (independent watchdog and window watchdog)

- SysTick: 64-bit counter
- **4-group UART: Support LIN and ISO7816**
- **1 I2C interface: Support SMBus/PMBus**
- **1 SPI interface**
- **USB2.0 full-speed controller and PHY:**
- Support USB Host and USB Device
- **USB PD and Type C controller and PHY**
- **Fast GPIO port**
- 69 I/O ports, with 24 external interrupts
- **Security features: Chip unique ID**
- **Debug mode: 2-wire serial debug interface (SDI)**
- **Package: LQFP, QFN, QSOP**

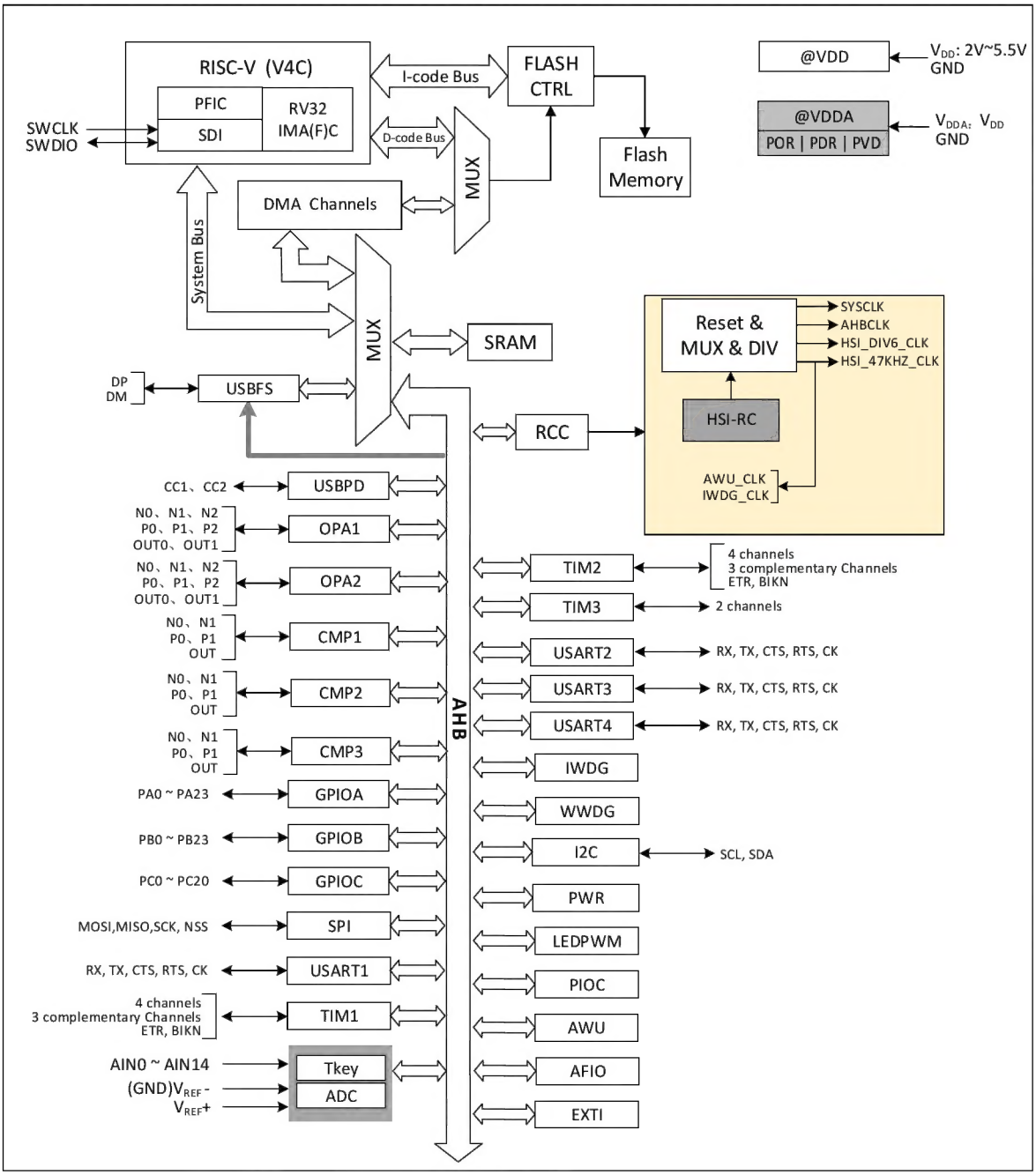
Model	Flash	RAM	GPIO	Advanced-control timer	General-purpose timer	RGB LED PWM	USART	Watchdog	USB Host Dev	USB PD typeC	ADC	OPA	CMP	Capacitive Touchkey	SPI	PIOC 1-wire interface	Package Form
CH643W	62K	20K	69	2	1	48×18	4	2	√	√	15+1	2	3	15-channel	√	√	QFN80
CH643Q	62K	20K	60	2	1	48×10	4	2	√	√	14+1	2	3	14-channel	√	√	LQFP64
CH643L	62K	20K	44	2	1	24×18	4	2	Dev	-	10+1	2	3	10-channel	√	√	LQFP48
CH643U	62K	20K	26	2	1	16×8	4	2	Dev	-	9+1	2	-	9-channel	√	√	QSOP28

Chapter 1 Specification Information

1.1 System Structure

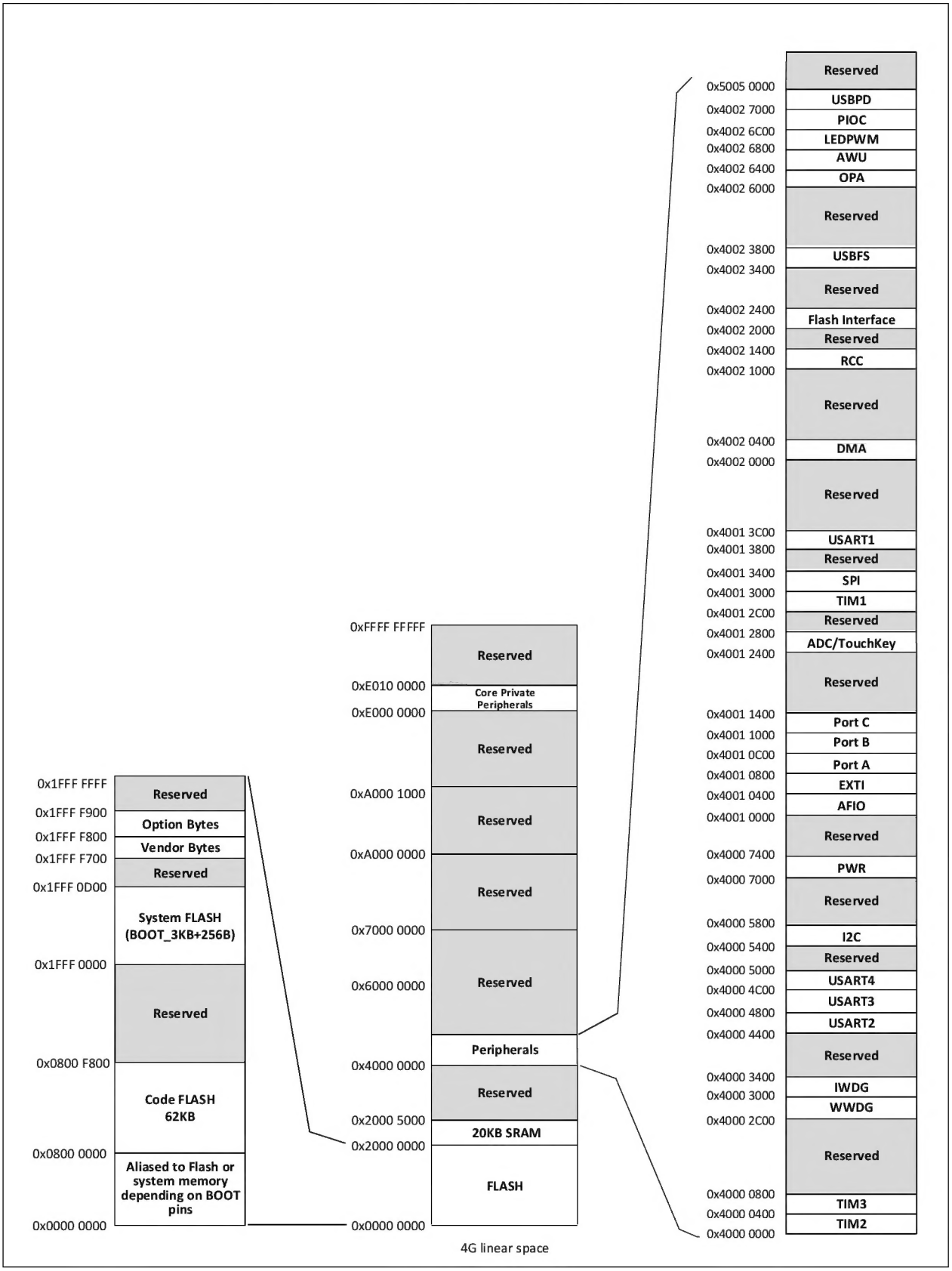
The microcontroller is designed on the basis of the RISC-V instruction set, and its architecture integrates QingKe microprocessor core, arbitration unit, DMA module, SRAM storage and other components through multiple bus groups to achieve interaction. A general-purpose DMA controller is integrated to reduce the CPU load and improve access efficiency, and a multi-level clock management mechanism is applied to reduce the power consumption of peripherals. The following diagram shows the overall internal architecture of the series chip.

Figure 1-1 System Block Diagram



1.2 Memory Map

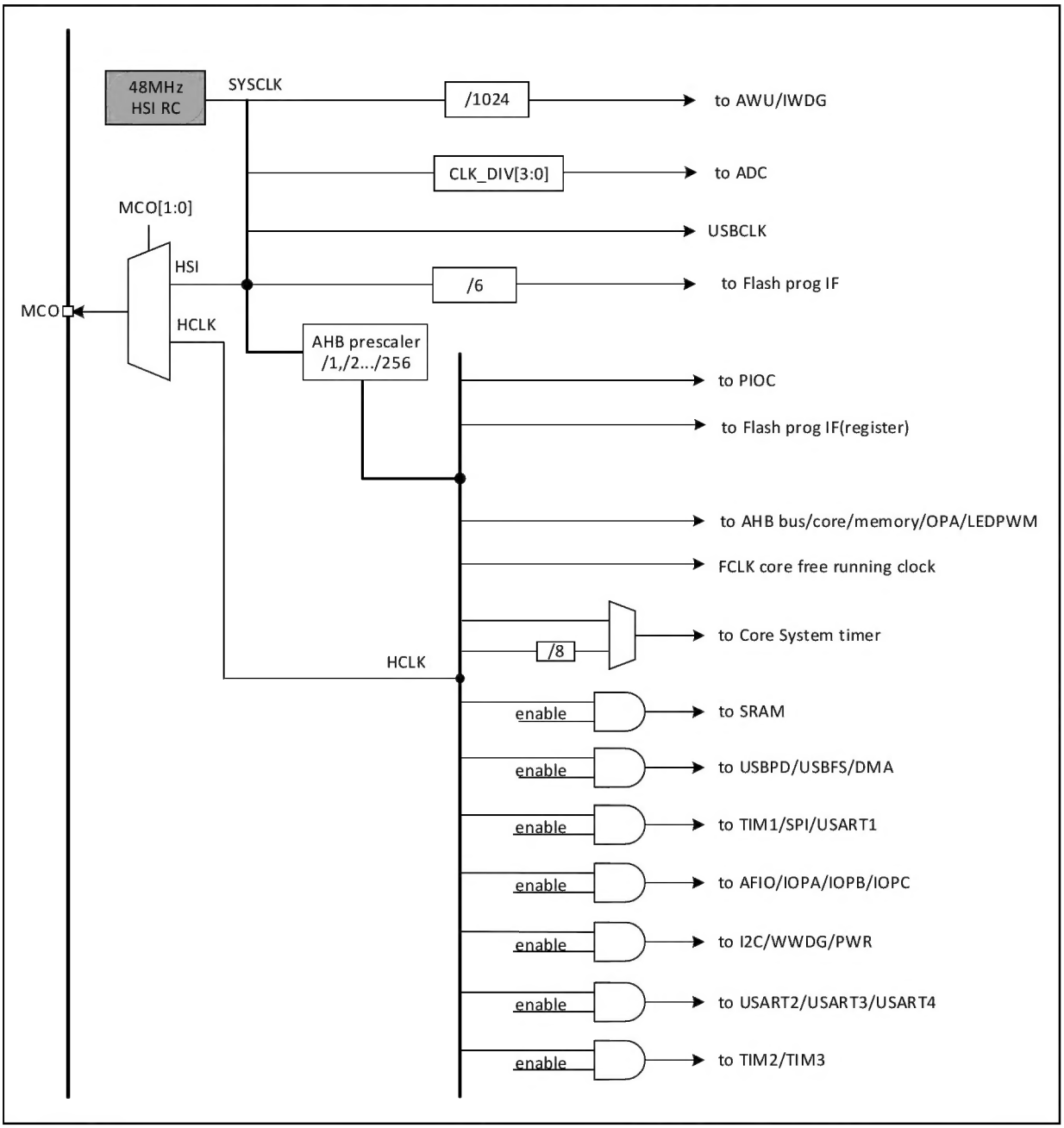
Figure 1-2 Memory address map



1.3 Clock Tree

System clock source: Internal high frequency RC oscillator (HSI)

Figure 1-3 Clock Tree Block Diagram



1.4 Functional Description

1.4.1 QingKe RISC-V4C Processor

RISC-V4C supports the IMAC subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as a fast programmable interrupt controller (PFIC), memory protection, branch prediction mode and extended instruction support. Externally multiple buses are connected to external unit modules, enabling interaction between external function modules and the core.

The processor with its minimal instruction set, multiple operating modes, and modular custom extensions can be flexibly applied to different scenarios of microcontroller design, such as small area low power embedded scenarios, high performance application operating system scenarios, etc.

- Support machine and user privileged modes
- Fast Programmable Interrupt Controller (PFIC)
- Multi-level hardware interrupt stack
- 2-wire serial debug interface (SDI)
- Standard memory protection design
- Static or dynamic branch prediction, efficient jumping, conflict detection mechanisms
- Custom extension instructions

1.4.2 Programmable Protocol I/O Controller (PIOC)

Programmable protocol I/O controller is based on a single clock cycle dedicated compact instruction set RISC core running at system mains frequency with 2K instruction program ROM and 49 SFR registers and PWM timer/counter, supporting protocol control of 2 I/O pins.

- Multiplex 4K bytes of system SRAM as a 2K word capacity program ROM, supporting program pause and dynamic loading.
- Provide 33 bytes of 1 register each in bidirectional and unidirectional mode, providing 6 levels of independent stacking.
- Support 1- and 2-wire interfaces with multiple protocol specifications by dynamically loading different protocol programs.

1.4.3 On-chip Memory

Built-in 20K bytes SRAM area for data storage and data loss after power failure. 4K of which can be used for PIOC.

Built-in 62K bytes of program flash memory storage (Code FLASH) for user applications and constant data storage.

3328 bytes of internal system memory (System FLASH) for system bootloader storage with built-in bootloader.

256 bytes for system non-volatile configuration information storage and 256 bytes for user selectable word storage.

1.4.4 Power Supply Scheme

- V_{DD} = 2 ~ 5.5V: supplies power to the I/O pins and internal regulator.
- V_{DDA} = 2 ~ 5.5V: supplies the high frequency RC oscillator, the analogue part of the ADC. The V_{DDA} voltage must be the same as the V_{DD} voltage. When using the ADC, V_{DDA} should be no less than 2.5V.

1.4.5 Power Supply Monitor

A power-on reset (POR)/power-down reset (PDR) circuit is integrated inside the chip, which is always active and ensures that the system operates when the supply exceeds 2V; when VDD falls below the set threshold ($V_{POR/PDR}$), the device is placed in reset without the need for an external reset circuit.

In addition the system has a programmable voltage monitor (PVD), which needs to be switched on by software, to

compare the voltage magnitude of the V_{DD} supply with the set threshold value V_{PVD}. Turning on the PVD corresponding edge interrupt allows interrupt notifications to be received when V_{DD} drops to the PVD threshold or rises to the PVD threshold. For the values of $V_{POR/PDR}$ and V_{PVD} refer to chapter 3.

1.4.6 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are two modes of operation depending on the application mode.

- On mode: normal running operation, providing stable core power.
- Low-power mode: low-power operation of the regulator when the CPU is in Standby mode.

1.4.7 Low-power Mode

The system supports 3 low-power modes, which can be selected to achieve the best balance for conditions such as low-power consumption, short start-up times and multiple wake-up events.

- Sleep mode

In Sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in working condition. This mode is the shallowest low-power mode, but the fastest wake-up can be achieved.
Exit condition: any interrupt or wake-up event.

- Stop mode

This mode puts the FLASH into low-power mode and the RC oscillator of the HSI is switched off.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on RST, IWDG reset, where EXTI signal includes one of the 24 external I/O ports, output of PVD, wake-up signal of USB, wake-up signal of USB PD, etc.

- Standby mode

This mode FLASH enters low-power mode, the RC oscillator of HSI is switched off and the system LDO enters low-power mode.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on RST, IWDG reset, where EXTI signal includes one of the 24 external I/O ports, the output of PVD, wake-up signal of USB, wake-up signal of USB PD, etc.

1.4.8 Fast Programmable Interrupt Controller (PFIC)

The chip has a built-in Fast Programmable Interrupt Controller (PFIC) that supports up to 255 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. Currently the chip manages 7 core private interrupts and 39 peripheral interrupt management, with other interrupt sources reserved. the PFIC registers are all accessible in both user and machine privileged modes.

- 2 individually maskable interrupts
- Provide one non-maskable interrupt NMI
- Support hardware interrupt stack (HPE) without instruction overhead
- Provide 4 table-free interrupts (VTF) for faster access to interrupt service routines
- Vector table support address or instruction mode
- Interrupt nesting depth can be configured up to 2 levels
- Support interrupt tail linking

1.4.9 External Interrupt/event Controller (EXTI)

The external interrupt/event controller contains a total of 28 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and

can be individually masked; a pending register maintains the status of all interrupt requests. Up to 69 general purpose I/O ports are optionally connected to 24 external interrupt lines.

1.4.10 General DMA Controller

The system has a built-in general purpose DMA controller that manages 8 channels to flexibly handle high-speed data transfers between memory to memory, peripheral to memory and memory to peripheral, supporting the ring buffer approach. Each channel has dedicated hardware DMA request logic to support one or more peripheral access requests to memory, with configurable access priority, transfer length, source and destination addresses for transfers, etc.

DMA is used for the main peripherals including: General-purpose/advanced-control timers TIMx, ADC, USART, I2C, SPI.

USB and USB PD have additional dedicated independent DMA channels.

Note: DMA and CPU access to system SRAM after arbiter arbitration.

1.4.11 Clock and Boot

The system clock source HSI is turned on by default, and the internal 48MHz RC oscillator 6 division is used as the default CPU clock when no clock is configured or after a reset. For low power modes where the clock is turned off, the system will first turn on the internal RC oscillator upon wake-up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

1.4.12 Analog-to-digital Converter (ADC) and Touchkey Capacitance Detection (TKey)

The chip has an embedded 12-bit analog/digital converter (ADC) providing up to 15 external channels and one internal channel sample, with programmable channel sample times for single, continuous, sweep or intermittent conversion. The provision of an analogue watchdog function allows very accurate monitoring of one or more selected channels for monitoring channel signal voltages. Supports external event-triggered transitions, with trigger sources including internal signals from the on-chip timer and external pins. Supports the use of DMA operation.

ADC internal channels are internal reference supply voltage sampling channels.

Touch key capacitance detection unit, providing up to 15 detection channels, multiplexes the external channels of the ADC module. The detection results are converted to output results by the ADC module, and the touch key status is identified by the touch detection algorithm subroutine library or by user software.

Note: The channel 3, channel 7, channel 11 and channel 15 functions of the ADC are not available for products with a lot number with the penultimate 5 digits being 0.

1.4.13 Timer and Watchdog

- Advanced-control timer (TIM1, TIM2)

Advanced-control timer is a 16-bit auto-loading incremental/decremental counter with a 16-bit programmable prescaler. In addition to the full general purpose timer functions, it can be seen as a 3-phase PWM generator allocated to 6 channels, has a complementary PWM output function with deadband insertion, allows the timer to be updated for repeated count cycles after a specified number of counter cycles, a brake function, etc. Many of the functions of the Advanced Control Timer are identical to those of the General Purpose Timer and the internal architecture is the same, therefore the Advanced Control Timer can operate in concert with other TIM timers via the timer link function, providing synchronization or event link functionality.

- General-purpose timer (TIM3)

The general-purpose timer is a 16-bit auto-loading recursive counter with a programmable 16-bit prescaler and 2

independent channels, each supporting input capture, output comparison, PWM generation and single pulse mode output. It can also work with advanced control timers via the timer linking function to provide synchronous or event linking functionality. In debug mode, the counter can be frozen and any general-purpose timer can be used to generate PWM outputs.

- Independent watchdog

The Independent Watchdog is a free-running 12-bit decrementing counter supporting 7 division factors. The clock source is provided by the division of the (HSI/1024) clock. IWDG works completely independently of the main program and can therefore be used to reset the entire system in case of problems or as a free timer to provide timeout management for applications. With the option byte it can be configured to be a software or hardware start watchdog. In debug mode, the counter can be frozen.

- Window watchdog

Window watchdog is a 7-bit decrementing counter and can be set to run freely. It can be used to reset the entire system in the event of a problem. It is driven by the master clock and has an early warning interrupt function; in debug mode the counter can be frozen.

- SysTick timer

QingKe microprocessor core comes with a 64-bit optional incremental or decremental counter for generating SYSTICK exceptions (exception number: 12), which can be used exclusively in real time operating systems to provide a "heartbeat" rhythm for the system, or as a standard 64-bit counter. Automatic reload function and programmable clock source.

1.4.14 Communication Interface

1.4.14.1 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The chip provides 4 sets of universal synchronous/asynchronous transceivers. It supports full duplex asynchronous serial communication, synchronous unidirectional communication as well as half duplex single line communication, also LIN (Local Interconnect Network), ISO7816 compatible smart card protocol and IrDA SIR ENDEC transmission codec specification, as well as modem (CTS/RTS hardware flow control) operation, and also supports multi-processor communication. It uses a fractional baud rate generator system and supports continuous communication by DMA operation.

1.4.14.2 Serial Peripheral Interface (SPI)

The chip provides 1 serial peripheral SPI interface, support master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

1.4.14.3 I2C Bus

The chip provides one I2C bus interface, capable of working in multi-master or slave mode, performing all I2C bus specific timing, protocols, arbitration, etc. Both standard and fast communication speeds are supported and it is also compatible with SMBus 2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0/PMBus bus.

Note: I2C function is not available for products with a 0 in the penultimate 5 digits of the batch number.

1.4.14.4 Universal Serial Bus USB2.0 Full-speed Host/Device Controller (USBFS)

USB2.0 Full-speed Host Controller and Device Controller (USBFS) following the USB2.0 Full-speed standard and supporting the BC charging protocol. Provides 8 configurable USB device endpoints and a set of host endpoints. Supports control/lot/sync/interrupt transfers, double buffer mechanism, USB bus hang/resume operation and provides standby/wakeup functions. 48MHz clock dedicated to the USBFS module is generated directly from the internal high-speed clock (HSI).

1.4.14.5 USB PD and type C Controller (USB PD)

Built-in USB Power Delivery controller and PD transceiver PHY, support for USB type-C master-slave detection, automatic BMC codec and CRC, hardware edge control, support for USB PD2.0 and PD3.0 power delivery control, support for fast charging, support for PD powered and PD powered end applications.

1.4.15 General-purpose Input and Output (GPIO)

The system provides 3 groups of GPIO ports with a total of 69 GPIO pins. Each pin can be configured by software as an output, input (with or without pull-up, some pins support pull-down) or multiplexed peripheral function port. All GPIO pins support controlled pull-up, only PA0-PA15 and PC16-PC17 support controlled pull-down, the remaining pins do not support pull-down. PC14-PC17 support multiple pull-up modes, set by dedicated control registers corresponding to the PD and USB pins respectively.

Most GPIO pins are shared with either digital or analogue multiplexed peripherals. All PA and PB GPIO pins have high current drive capability with simple constant current functionality and all support PWM. a lockout mechanism is provided to freeze the I/O configuration to avoid accidental writes to I/O registers.

Most of the I/O pins in the system are powered by V_{DD}, and changing the V_{DD} power supply will change the I/O pin output level high enough to adapt to the external communication interface level. Please refer to the pin description for specific pins.

1.4.16 Operational Amplifier/Comparator (OPA)

The chip has a built-in 2-group op-amp (OPA), which can also be used as a voltage comparator. Its input can be selected for multiple channels by changing the configuration, including amplification selection for the programmable gain op-amp (PGA), and its output can be selected for 2 channels by changing the configuration, internally associated to ADC channels. External analogue small signal amplification is supported for feeding into the ADC for small signal ADC conversion.

1.4.17 Voltage Comparator (CMP)

The chip has 3 built-in rail-to-rail analog voltage comparators with optional hysteresis characteristics. The voltage comparison results are triggered by the GPIO output or internally directly into the input channels CH1 to CH3 of the TIM2.

1.4.18 RGB Tri-colour LED Pulse Width Modulation PWM Driver (LEDPWM)

The chip has a built-in 3*16=48 channel PWM current driver, supports multiple COM common terminal dynamic scanning, can be used for RGB tri-colour or monochrome LED dot matrix display driver. Optional 7-bit or 8-bit valid PWM data, supports up to 3*8-bit colour PWM supporting 16777216 combined colours; optional 6-bit or 7-bit or 8-bit luminance PWM supporting 256 levels of greyscale; fade time adjustable in multiple steps, supports luminance PWM repeat group frame, supports 1/2 to 1/18 or more COM dynamic scanning; dedicated DMA mode

supports loading from Flash-ROM The dedicated DMA mode supports loading of pre-set cured data from Flash-ROM or loading of edited display data from RAM.

The CH643 can support both LED matrix dynamic display drive and keyboard matrix scan detection, both LED matrix and keyboard matrix are driven by PWM channel pins as column, LED matrix supports up to 3*16=48 columns, keyboard matrix supports up to 16 columns.

LED row drive by the common terminal COM dynamic time scan, COM drive in two ways: fully built-in way, external PMOS way.

The fully built-in method is peripherally compact and low cost, with the COM pin internal NMOS directly driving the sink fill current as the line scan, while the PWM channel is connected to the LED anode by the internal PMOS providing the source current. Usually, the PA pin is used as PWM and the PB pin is used as COM.

The external PMOS approach supports higher current and higher brightness, with the COM pin controlling the external P-type MOSFET providing the source current for line scan respectively, and the PWM channel with the internal NMOS providing the sink source current to the LED cathode. Typically, the PB pin as well as the PA pin are used as PWM, with the PC pin and the remaining pins controlling external P-type MOSFETs respectively.

The keyboard matrix supports the same number of COMs as the LED matrix as line scan outputs. The fully internal mode is provided by PA0-15 series resistors as current mode column sampling inputs with active sink current; the external PMOS mode is provided by PB0-15 series resistors as current mode column sampling inputs with active source current. Current mode key detection reuses the LED display driver pins without the need for additional GPIOs; the CH643 also supports conventional voltage mode key detection using multiple additional GPIO pins as column sampling inputs.

All PA pins have source current simple constant current function, sink current simple constant current function; all PB pins have sink current simple constant current function, as a fully built-in COM driver with large sink current driving capability.

The CH643 chip supports the following matrix combinations.

LED matrix	PWM pin mode	PWM channel Pin name	PWM channel LED columns	Keyboard columns	COM number line scan	CH 643W	CH 643Q	CH 643L	CH 643U	COM method Peripherals
Monochrome	PA16I	PA0-15	16	16	8	√	√	√	√	Fully built-in
RGB	PA15	PA0-4, PA6-15	3*5=15	15	8	√	√	√	√	Fully built-in
Monochrome	PA16I	PA0-15	16	16	18	√	√	√		Fully built-in
RGB/ Monochrome	PA24	PA0-23	3*8=24	16	18	√	√	√		Fully built-in
RGB/ Monochrome	PB16PA8	PB0-15, PA16-23	3*8=24	16	18*PMOS	√	√	√		External PMOS
RGB/ Monochrome	PA24	PA0-23	3*8=24	None	18*PMOS	√	√	√		External PMOS
RGB/ Monochrome	PA24	PA0-23	3*8=24	16	24	√	√			Fully built-in
RGB/ Monochrome	PB24	PB0-23	3*8=24	16	32*PMOS	√	√			External PMOS
RGB/ Monochrome	PA24PB24	PA0-23, PB0-23	3*16=48	16	10*PMOS	√	√			External PMOS

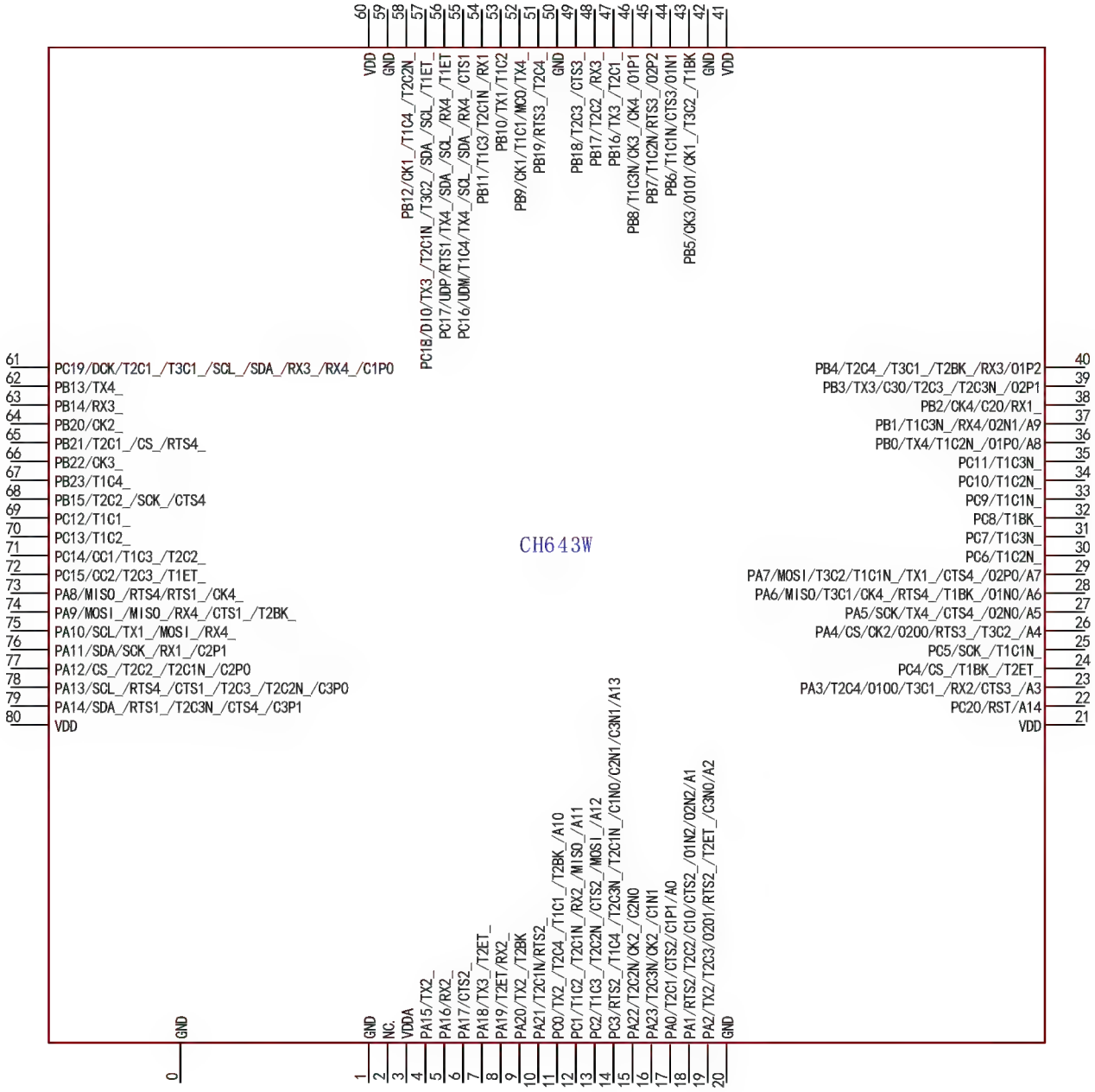
RGB/ Monochrome	PA24PB24	PA0-23, PB0-23	3*16=48	16	18*PMOS	√				External PMOS

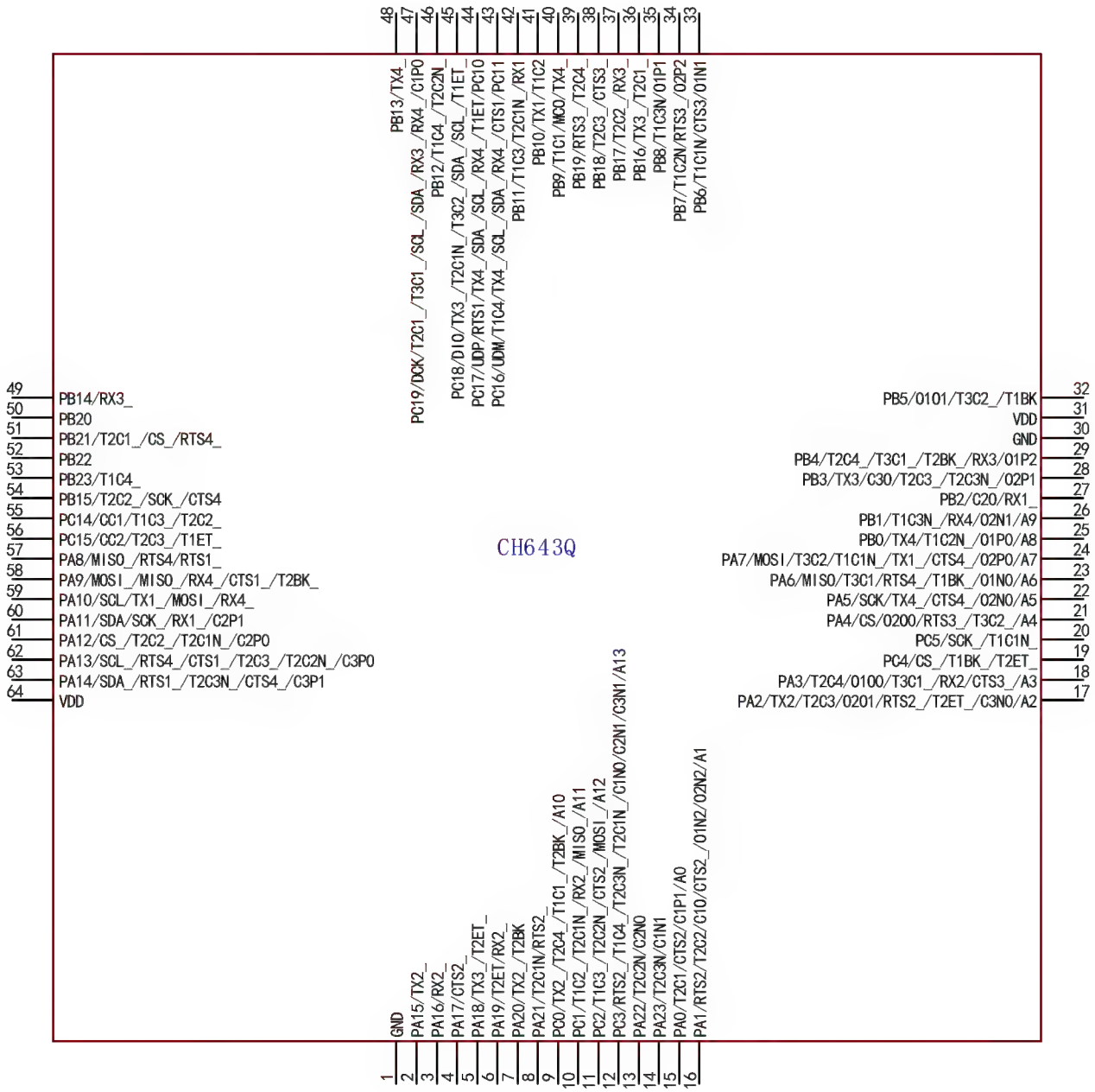
1.4.19 2-wire SDI Serial Debug Interface

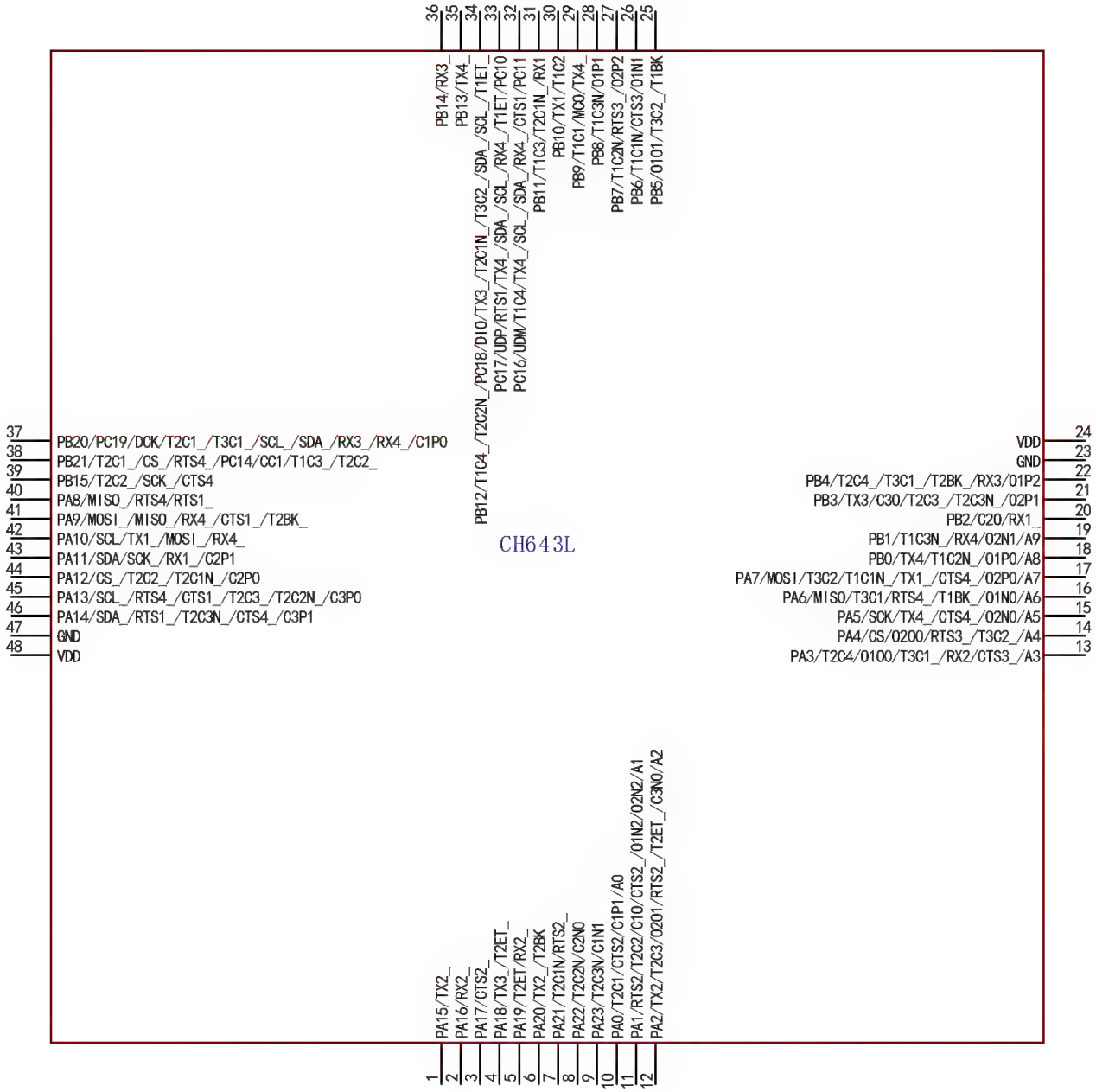
The core comes with a 2-wire serial debug interface (SDI) including the SWDIO and SWCLK pins. The default debug interface pin function is turned on after system power-up or reset, and the SDI can be turned off as required after the main program is running.

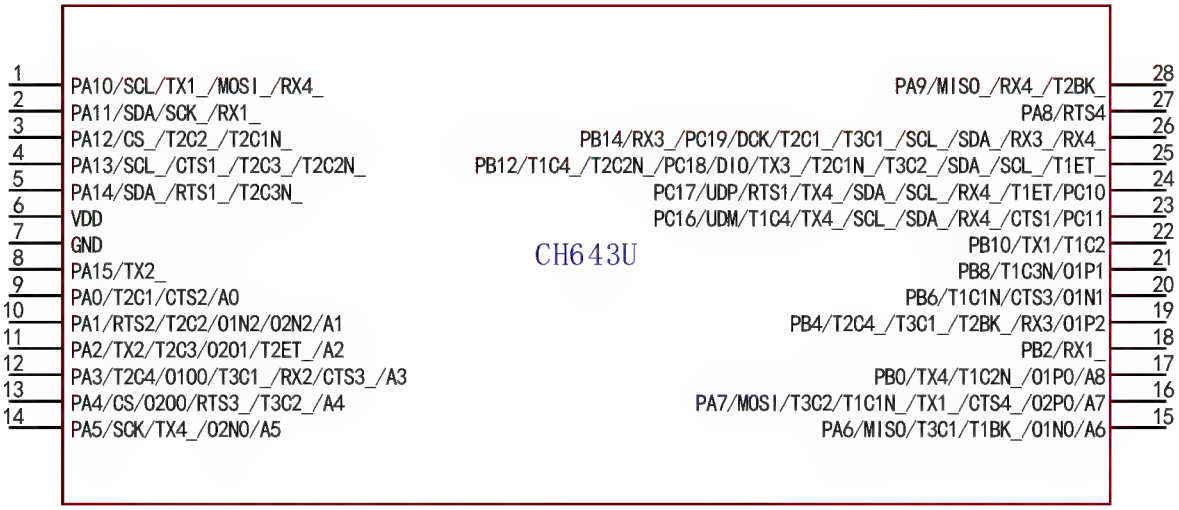
Chapter 2 Pinouts and Pin Definition

2.1 Pinouts




CH643Q
1 GND
2 PA15/TX2_
3 PA16/RX2_
4 PA17/CTS2_
5 PA18/TX3_/T2ET_
6 PA19/T2ET/RX2_
7 PA20/TX2_/T2BK
8 PA21/T2C1N/RTS2_
9 PC0/TX2_/T2C4_/T1C1_/T2BK_/A10
10 PC1/T1C2_/T2C1N_/RX2_/MISO_/A11
11 PC2/T1C3_/T2C2N_/CTS2_/MOSI_/A12
12 PC3/RTS2_/T1C4_/T2C3N_/T2C1N_/C1NO/C2N1/C3N1/A13
13 PA22/T2C2N/C2NO
14 PA23/T2C3N/C1N1
15 PA0/T2C1/CTS2/C1P1/A0
16 PA1/RTS2/T2C2/C1O/CTS2_/O1N2/O2N2/A1
17 PA2/TX2/T2C3/O2O1/RTS2_/T2ET_/C3NO/A2
18 PA3/T2C4/O1OO/T3C1_/RX2/CTS3_/A3
19 PC4/CS_/T1BK_/T2ET_
20 PC5/SCK_/T1C1N_
21 PA4/CS/O2OO/RTS3_/T3C2_/A4
22 PA5/SCK/TX4_/CTS4_/O2NO/A5
23 PA6/MISO/T3C1/RTS4_/T1BK_/O1NO/A6
24 PA7/MOSI/T3C2/T1C1N_/TX1_/CTS4_/O2PO/A7
25 PB0/TX4/T1C2N_/O1PO/A8
26 PB1/T1C3N_/RX4/O2N1/A9
27 PB2/C2O/RX1_
28 PB3/TX3/C3O/T2C3_/T2C3N_/O2P1
29 PB4/T2C4_/T3C1_/T2BK_/RX3/O1P2
30 GND
31 VDD
32 PB5/O1O1/T3C2_/T1BK
33 PB6/T1C1N/CTS3/O1N1
34 PB7/T1C2N/RTS3_/O2P2
35 PB8/T1C3N/O1P1
36 PB16/TX3_/T2C1_
37 PB17/T2C2_/RX3_
38 PB18/T2C3_/CTS3_
39 PB19/RTS3_/T2C4_
40 PB9/T1C1/MCO/TX4_
41 PB10/TX1/T1C2
42 PB11/T1C3/T2C1N_/RX1
43 PC16/UDM/T1C4/TX4_/SCL_/SDA_/RX4_/CTS1/PC11
44 PC17/UDP/RTS1/TX4_/SDA_/SCL_/RX4_/T1ET/PC10
45 PC18/DIO/TX3_/T2C1N_/T3C2_/SDA_/SCL_/T1ET_
46 PB12/T1C4_/T2C2N_
47 PC19/DCK/T2C1_/T3C1_/SCL_/SDA_/RX3_/RX4_/C1PO
48 PB13/TX4_
49 PB14/RX3_
50 PB20
51 PB21/T2C1_/CS_/RTS4_
52 PB22
53 PB23/T1C4_
54 PB15/T2C2_/SCK_/CTS4
55 PC14/CC1/T1C3_/T2C2_
56 PC15/CC2/T2C3_/T1ET_
57 PA8/MISO_/RTS4/RTS1_
58 PA9/MOSI_/MISO_/RX4_/CTS1_/T2BK_
59 PA10/SCL/TX1_/MOSI_/RX4_
60 PA11/SDA/SCK_/RX1_/C2P1
61 PA12/CS_/T2C2_/T2C1N_/C2PO
62 PA13/SCL_/RTS4_/CTS1_/T2C3_/T2C2N_/C3PO
63 PA14/SDA_/RTS1_/T2C3N_/CTS4_/C3P1
64 VDD


CH643L
1 PA15/TX2_
2 PA16/RX2_
3 PA17/CTS2_
4 PA18/TX3_/T2ET_
5 PA19/T2ET/RX2_
6 PA20/TX2_/T2BK
7 PA21/T2C1N/RTS2_
8 PA22/T2C2N/C2N0
9 PA23/T2C3N/C1N1
10 PA0/T2C1/CTS2/C1P1/A0
11 PA1/RTS2/T2C2/C10/CTS2_/01N2/02N2/A1
12 PA2/TX2/T2C3/0201/RTS2_/T2ET_/C3N0/A2
13 PA3/T2C4/0100/T3C1_/RX2/CTS3_/A3
14 PA4/CS/0200/RTS3_/T3C2_/A4
15 PA5/SCK/TX4_/CTS4_/02N0/A5
16 PA6/MISO/T3C1/RTS4_/T1BK_/01N0/A6
17 PA7/MOSI/T3C2/T1C1N_/TX1_/CTS4_/02P0/A7
18 PB0/TX4/T1C2N_/01P0/A8
19 PB1/T1C3N_/RX4/02N1/A9
20 PB2/C20/RX1_
21 PB3/TX3/C30/T2C3_/T2C3N_/02P1
22 PB4/T2C4_/T3C1_/T2BK_/RX3/01P2
23 GND
24 VDD
25 PB5/0101/T3C2_/T1BK
26 PB6/T1C1N/CTS3/01N1
27 PB7/T1C2N/RTS3_/02P2
28 PB8/T1C3N/01P1
29 PB9/T1C1/MC0/TX4_
30 PB10/TX1/T1C2
31 PB11/T1C3/T2C1N_/RX1
32 PC16/UDM/T1C4/TX4_/SCL_/SDA_/RX4_/CTS1/PC11
33 PC17/UDP/RTS1/TX4_/SDA_/SCL_/RX4_/T1ET/PC10
34 PB12/T1C4_/T2C2N_/PC18/DIO/TX3_/T2C1N_/T3C2_/SDA_/SCL_/T1ET_
35 PB13/TX4_
36 PB14/RX3_
37 PB20/PC19/DCK/T2C1_/T3C1_/SCL_/SDA_/RX3_/RX4_/C1P0
38 PB21/T2C1_/CS_/RTS4_/PC14/CC1/T1C3_/T2C2_
39 PB15/T2C2_/SCK_/CTS4
40 PA8/MISO_/RTS4/RTS1_
41 PA9/MOSI_/MISO_/RX4_/CTS1_/T2BK_
42 PA10/SCL/TX1_/MOSI_/RX4_
43 PA11/SDA/SCK_/RX1_/C2P1
44 PA12/CS_/T2C2_/T2C1N_/C2P0
45 PA13/SCL_/RTS4_/CTS1_/T2C3_/T2C2N_/C3P0
46 PA14/SDA_/RTS1_/T2C3N_/CTS4_/C3P1
47 GND
48 VDD



Note: The alternate functions in the pin diagram are abbreviated.

Example: A: ADC_ (A10:ADC_IN10)

C: CMP_ (C3N0:CMP3_N0, C3O:CMP3_OUT)

T: TIME_ (T2C4:TIM2_CH4, T2C2N:TIM2_CH2N)

O: OPA_ (O1N2:OPA1_N2, O2O0:OPA2_OUT0)

TX2/RX2:USART2_TX/ USART2_RX

CS: SPI_NSS

UDP: USBDP

UDM: USBDM

DIO: SWDIO

DCK: SWCLK

2.2 Pin Description

Table 2-1 Pin definitions

Note that the pin function descriptions in the table below are for all functions and do not refer to specific chip models. Peripheral resources may vary from model to model, so please check the availability of this function against the chip model resource table before viewing.

Pin				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
QFN80	LQFP64	LQFP48	QSOP28					
0	-	-	-	GND	P	GND		
1	1	23	7	GND	P	GND		
2	-	-	-	NC.	-			
3	-	-	-	V_{DDA}	P	V_{DDA}		
4	2	1	8	PA15	I/O	PA15		TX2_2/TX2_4
5	3	2	-	PA16	I/O	PA16		RX2_2/RX2_4
6	4	3	-	PA17	I/O	PA17		CTS2_2/CTS2_4
7	5	4	-	PA18	I/O	PA18		TX3_2/T2ET_1/T2ET_3
8	6	5	-	PA19	I/O	PA19	T2ET	RX2_1/T2ET_2
9	7	6	-	PA20	I/O	PA20	T2BK	TX2_1/T2BK_2
10	8	7	-	PA21	I/O	PA21	T2C1N	RTS2_2
11	9	-	-	PC0	I/O/A	PC0	A10	TX2_3/T2C4_5 /T2C4_6/T1C1_3/T2BK_4
12	10	-	-	PC1	I/O/A	PC1	A11(3)	T1C2_3/T2C1N_4/RX2_3/MISO_3
13	11	-	-	PC2	I/O/A	PC2	A12	T1C3_3/T2C2N_4/CTS2_3/MOSI_3
14	12	-	-	PC3	I/O/A	PC3	C1N0/C2N1/C3N1/A13	RTS2_3/T1C4_3 /T2C3N_4/T2C1N_2/RTS2_4
15	13	8	-	PA22	I/O/A	PA22	T2C2N/C2N0	CK2_2/T2C2N_2/CK2_4
16	14	9	-	PA23	I/O/A	PA23	T2C3N/C1N1	CK2_1/T2C3N_2
17	15	10	9	PA0	I/O/A	PA0	T2C1/CTS2 /C1P1/A0	T2C1_2
18	16	11	10	PA1	I/O/A	PA1	RTS2/T2C2/C1O /O1N2/O2N2/A1	CTS2_1/T2C2_2
19	17	12	11	PA2	I/O/A	PA2	TX2/T2C3/O2O1/C3N0/A 2	RTS2_1/T2ET_5 /T2C3_1/T2ET_6
20	30	47	-	GND	P	GND		
21	31	24	6	V_{DD}	P	V_{DD}		
22	-	-	-	PC20	I/O/A	PC20	RST/A14	
23	18	13	12	PA3	I/O/A	PA3	RX2/T2C4/O1O0/A3(3)	T3C1_3/T2C4_1/CTS3_2
24	19	-	-	PC4	I/O	PC4		CS_3/T1BK_3/T2ET_4
25	20	-	-	PC5	I/O	PC5		SCK_3/T1C1N_3
26	21	14	13	PA4	I/O/A	PA4	CS/CK2/O2O0/A4	RTS3_2/T3C2_3

Pin				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
QFN80	LQFP64	LQFP48	QSOP28					
27	22	15	14	PA5	I/O/A	PA5	SCK/O2N0/A5	TX4_1/CTS4_4
28	23	16	15	PA6	I/O/A	PA6	MISO/T3C1/O1N0/A6	CK4_1/RTS4_4/T1BK_1
29	24	17	16	PA7	I/O/A	PA7	MOSI/T3C2/O2P0/A7(3)	T1C1N_1/TX1_3/CTS4_1
30	-	-	-	PC6	I/O	PC6		T1C2N_3
31	-	-	-	PC7	I/O	PC7		T1C3N_3/PIOC_IO0_1
32	-	-	-	PC8	I/O	PC8		T1BK_4
33	-	-	-	PC9	I/O	PC9		T1C1N_4
34	44	33	24	PC10(4)	I/O	PC10		T1C2N_4
35	43	32	23	PC11(5)	I/O	PC11		T1C3N_4
36	25	18	17	PB0	I/O/A	PB0	TX4/O1P0/A8	T1C2N_1
37	26	19	-	PB1	I/O/A	PB1	RX4/O2N1/A9	T1C3N_1
38	27	20	18	PB2	I/O/A	PB2	CK4/C2O	RX1_3/CK4_2/CK4_5
39	28	21	-	PB3	I/O/A	PB3	TX3/C3O/O2P1	T2C3_2/T2C3N_5 /T2C3_3/T2C3N_6
40	29	22	19	PB4	I/O/A	PB4	RX3/O1P2	T2C4_2/T3C1_1 /T2BK_5/T2C4_3/T2BK_6
41	64	48	-	V_{DD}	P	V_{DD}		
42	-	-	-	GND	P	GND		
43	32	25	-	PB5	I/O/A	PB5	CK3/O1O1/T1BK	CK1_2/T3C2_1/CK3_1/T1BK_2
44	33	26	20	PB6	I/O/A	PB6	T1C1N/CTS3/O1N1	T1C1N_2/CTS3_1
45	34	27	-	PB7	I/O/A	PB7	T1C2N/O2P2/RTS3	RTS3_1/T1C2N_2
46	35	28	21	PB8	I/O/A	PB8	T1C3N/O1P1	CK3_2/CK4_3/T1C3N_2
47	36	-	-	PB16	I/O	PB16		TX3_3/T2C1_4
48	37	-	-	PB17	I/O	PB17		T2C2_4/RX3_3
49	38	-	-	PB18	I/O	PB18		T2C3_4/CTS3_3
50	-	-	-	GND	P	GND		
51	39	-	-	PB19	I/O	PB19		RTS3_3/T2C4_4
52	40	29	-	PB9	I/O	PB9	CK1/T1C1/MCO	TX4_3/CK1_1/T1C1_1/T1C1_2
53	41	30	22	PB10	I/O	PB10	TX1/T1C2	T1C2_1/T1C2_2/TX1_2
54	42	31	-	PB11	I/O	PB11	T1C3/RX1	T1C3_1/T1C3_2/RX1_2/T2C1N_6
55	43	32	23	PC16(5)	I/O/A	PC16	UDM/T1C4/CTS1	TX4_2/SCL_2(3)/SDA_4(3)/RX4_5 /CTS1_1/T1C4_1
56	44	33	24	PC17(4)	I/O/A	PC17	UDP/RTS1/T1ET	TX4_5/SDA_2(3)/SCL_4(3)/RX4_2 /RTS1_1/T1ET_1
57	45	34	25	PC18(6)	I/O	PC18	DIO/PIOC_IO0_0	TX3_1/T2C1N_5/T3C2_2/SDA_3(3) /SCL_5(3)/T1ET_2/T1ET_3
58	46			PB12(6)	I/O	PB12		CK1_3/T1C4_2/T2C2N_5/T2C2N_6

Pin				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
QFN80	LQFP64	LQFP48	QSOP28					
59	-	-	-	GND	P	GND		
60	-	-	-	V_{DD}	P	V_{DD}		
61	47	37	26	PC19(7)	I/O/A	PC19	DCK/PIOC_IO1/C1P0	T2C1_5/T3C1_2/SCL_3(3)/SDA_5(3) /RX3_1/RX4_4/T2C1_6
62	48	35	-	PB13	I/O	PB13		TX4_4
63	49	36	26	PB14(7)	I/O	PB14		RX3_2
64	50	37	-	PB20(7)	I/O	PB20		CK2_3
65	51	38	-	PB21(8)	I/O	PB21		T2C1_1/CS_1/RTS4_1/T2C1_3
66	52	-	-	PB22	I/O	PB22		CK3_3
67	53	-	-	PB23	I/O	PB23		T1C4_4
68	54	39	-	PB15	I/O	PB15	CTS4	T2C2_1/SCK_1/T2C2_3/CTS4_2 /CTS4_5
69	-	-	-	PC12	I/O	PC12		T1C1_4
70	-	-	-	PC13	I/O	PC13		T1C2_4
71	55	38	-	PC14(8)	I/O/A	PC14	CC1	T1C3_4/T2C2_6
72	56	-	-	PC15	I/O/A	PC15	CC2	T2C3_6/T1ET_4
73	57	40	27	PA8	I/O	PA8	RTS4	RTS1_2/CK4_4/RTS4_2/RTS4_5 /MISO_1
74	58	41	28	PA9	I/O	PA9		MOSI_1/RX4_1/CTS1_2/MISO_2 /T2BK_1/T2BK_3
75	59	42	1	PA10	I/O	PA10	SCL(3)	TX1_1/MOSI_2/RX4_3
76	60	43	2	PA11	I/O/A	PA11	SDA(3)/C2P1	SCK_2/RX1_1
77	61	44	3	PA12	I/O/A	PA12	C2P0	CS_2/T2C2_5/T2C1N_1/T2C1N_3
78	62	45	4	PA13	I/O/A	PA13	C3P0	SCL_1(3)/RTS4_3/CTS1_3/T2C3_5 /T2C2N_1/T2C2N_3
79	63	46	5	PA14	I/O/A	PA14	C3P1	SDA_1(3)/RTS1_3/T2C3N_1/CTS4_3 /T2C3N_3
80	-	-	-	V_{DD}	P	V_{DD}		

The CH643 will optionally reuse some of its pins for PWM drive or COM dynamic scan drive when RGB LED PWM is enabled.

Pin name	Function name	Function description
PA0-PA7	RED0-RED7	RGB LED red PWM drive output, each can be independently enabled or disabled.
PB0-PB7	RED8-RED15	
PA8-PA15	GRE0-GRE7	RGB LED green PWM drive output, each can be independently enabled or disabled.
PB8-PB15	GRE8-GRE15	
PA16-PA23	BLU0-BLU7	RGB LED blue PWM drive output, each can be independently enabled or

PB16-PB23	BLU8-BLU15	disabled.
PC18-PC19	COM0-COM1	RGB LED Dynamic Scan COM common drive output, each can be independently enabled or disabled.
PA16-PA21	COM2-COM7	RGB LED Dynamic Scan COM common drive output, each can be independently enabled or disabled.
PB16-PB23	COM8-COM15	RGB LED Dynamic Scan COM common drive output, each can be independently enabled or disabled.
PB0-PB15	COM16-COM31	RGB LED Dynamic Scan COM common drive output, each can be independently enabled or disabled.
PA0-PA15	COM32-COM47	RGB LED Dynamic Scan COM common drive output, each can be independently enabled or disabled.
PC0-PC15	COM48-COM63	RGB LED Dynamic Scan COM common drive output, each can be independently enabled or disabled.

Note 1: Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output;

A = analog signal input or output; P = power supply.

Note 2: The value after the remapping function underline indicates the configuration value of the corresponding bit in the AFIO register. For example: TX2_2 indicates that the corresponding bit of the AFIO register is configured as 10b.

Note 3: The channel 3, channel 7, channel 11, channel 15 and I2C functions of the ADC are not applicable to products with a lot number with the penultimate bit 5 being 0.

Note 4: For CH643Q, CH643L, CH643U chips, PC10 and PC17 pins are shorted and sealed inside the chip, prohibiting both IOs from being configured for output function; in USB applications, PC10 pin should be configured for floating input mode (default value after reset).

Note 5: For CH643Q, CH643L and CH643U chips, PC11 and PC16 pins are shorted and sealed inside the chip, prohibiting both IOs from being configured for output function; in USB applications, PC11 pin should be configured for floating input mode (default value after reset).

Note 6: For CH643L and CH643U chips, PB12 and PC18 pins are shorted and sealed inside the chip, forbidding both IOs to be configured as output function.

Note 7: For CH643L chip, PB20 and PC19 pins are short-circuited inside the chip, prohibiting both IOs from being configured as output function; for CH643U chip, PB14 and PC19 pins are short-circuited inside the chip, prohibiting both IOs from being configured as output function.

Note 8: For CH643L chip, PB21 and PC14 pins are shorted and sealed inside the chip, prohibiting both IOs from being configured for output function.

2.3 Pin Alternate Functions

Note: The pin function in the table below refer to all functions and does not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 2-2 Pin alternate and remapping functions

Alternate / Pin	ADC	TIM1/2	TIM3	USART	CMP	SYS	I2C	SPI	USB	OPA	PIOC
PA0	A0	T2C1 T2C1_2		CTS2	C1P1						
PA1	A1	T2C2 T2C2_2		RTS2 CTS2_1	C1O					O1N2 O2N2	
PA2	A2	T2C3 T2C3_1 T2ET_5 T2ET_6		TX2 RTS2_1	C3N0					O2O1	
PA3	A3[1]	T2C4 T2C4_1	T3C1_3	RX2 CTS3_2						O1O0	
PA4	A4		T3C2_3	CK2 RTS3_2				CS		O2O0	
PA5	A5			TX4_1 CTS4_4				SCK		O2N0	
PA6	A6	TIBK_1	T3C1	CK4_1 RTS4_4				MISO		O1N0	
PA7	A7[1]	TIC1N_1	T3C2	CTS4_1 TX1_3				MOSI		O2P0	
PA8				RTS4 RTS1_2 CK4_4 RTS4_2 RTS4_5				MISO_1			
PA9		T2BK_1 T2BK_3		RX4_1 CTS1_2				MOSI_1 MISO_2			
PA10				TX1_1 RX4_3			SCL[1]	MOSI_2			
PA11				RX1_1	C2P1		SDA[1]	SCK_2			
PA12		T2C2_5 T2C1N_1 T2C1N_3			C2P0			CS_2			
PA13		T2C3_5 T2C2N_1 T2C2N_3		RTS4_3 CTS1_3	C3P0		SCL_1[1]				
PA14		T2C3N_1 T2C3N_3		CTS4_3 RTS1_3	C3P1		SDA_1[1]				
PA15				TX2_2 TX2_4							
PA16				RX2_2 RX2_4							
PA17				CTS2_2 CTS2_4							
PA18		T2ET_1 T2ET_3		TX3_2							
PA19		T2ET T2ET_2		RX2_1							
PA20		T2BK T2BK_2		TX2_1							
PA21		T2C1N		RTS2_2							
PA22		T2C2N T2C2N_2		CK2_2 CK2_4	C2NO						
PA23		T2C3N T2C3N_2		CK2_1	C1N1						
PB0	A8	T1C2N_1		TX4						O1P0	
PB1	A9	T1C3N_1		RX4						O2N1	
PB2				RX1_3 CK4 CK4_2 CK4_5	C2O						

Alternate / Pin	ADC	TIM1/2	TIM3	USART	CMP	SYS	I2C	SPI	USB	OPA	PIOC
PB3		T2C3_2 T2C3_3 T2C3N_5 T2C3N_6		TX3	C3O					O2P1	
PB4		T2C4_2 T2C4_3 T2BK_5 T2BK_6	T3C1_1	RX3						O1P2	
PB5		T1BK T1BK_2	T3C2_1	CK3 CK1_2 CK3_1						O1O1	
PB6		T1C1N T1C1N_2		CTS3 CTS3_1						O1N1	
PB7		T1C2N T1C2N_2		RTS3 RTS3_1						O2P2	
PB8		T1C3N T1C3N_2		CK3_2 CK4_3						O1P1	
PB9		T1C1 T1C1_1 T1C1_2		CK1 CK1_1 TX4_3		MCO					
PB10		T1C2 T1C2_1 T1C2_2		TX1 TX1_2							
PB11		T1C3 T1C3_1 T1C3_2 T2C1N_6		RX1 RX1_2							
PB12		T1C4_2 T2C2N_5 T2C2N_6		CK1_3							
PB13				TX4_4							
PB14				RX3_2							
PB15		T2C2_1 T2C2_3		CTS4 CTS4_2 CTS4_5				SCK_1			
PB16		T2C1_4		TX3_3							
PB17		T2C2_4		RX3_3							
PB18		T2C3_4		CTS3_3							
PB19		T2C4_4		RTS3_3							
PB20				CK2_3							
PB21		T2C1_1 T2C1_3		RTS4_1				CS_1			
PB22				CK3_3							
PB23		T1C4_4									
PC0	A10	T1C1_3 T2C4_5 T2C4_6 T2BK_4		TX2_3							
PC1	A11[1]	T1C2_3 T2C1N_4		RX2_3				MISO_3			
PC2	A12	T1C3_3 T2C2N_4		CTS2_3				MOSI_3			
PC3	A13	T1C4_3 T2C3N_4 T2C1N_2		RTS2_3 RTS2_4	C1NO C2N1 C3N1						
PC4		T1BK_3 T2ET_4						CS_3			
PC5		T1C1N_3						SCK_3			
PC6		T1C2N_3									
PC7		T1C3N_3									PIOC_IO0_1
PC8		T1BK_4									
PC9		T1C1N_4									
PC10		T1C2N_4									
PC11		T1C3N_4									
PC12		T1C1_4									

Alternate / Pin	ADC	TIM1/2	TIM3	USART	CMP	SYS	I2C	SPI	USB	OPA	PIOC
PC13		T1C2_4									
PC14		T1C3_4 T2C2_6							CC1		
PC15		T1ET_4 T2C3_6							CC2		
PC16		T1C4 T1C4_1		CTS1 CTS1_1 TX4_2 RX4_5			SCL_2(1) SDA_4(1)		UDM		
PC17		T1ET T1ET_1		RTS1 RTS1_1 RX4_2 TX4_5			SDA_2(1) SCL_4(1)		UDP		
PC18		T1ET_2 T1ET_3 T2C1N_5	T3C2_2	TX3_1		DIO	SDA_3(1) SCL_5(1)				PIOC_IO0_0
PC19		T2C1_5 T2C1_6	T3C1_2	RX3_1 RX4_4	C1P0	DCK	SCL_3(1) SDA_5(1)				PIOC_IO1
PC20	A14					RST					

Note: Channel 3, channel 7, channel 11, channel 15 and I2C functions of the ADC are not available for products with a lot number with a penultimate 5 digit of 0;

Chapter 3 Electrical Characteristics

3.1 Test Conditions

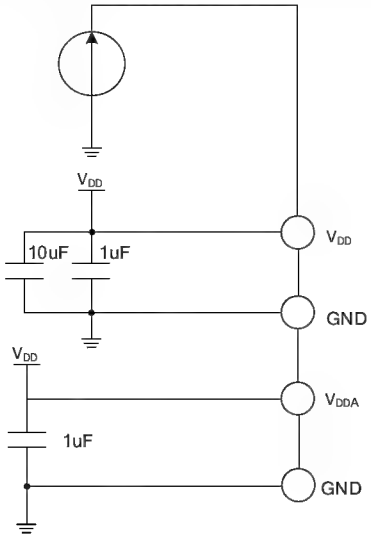
All voltages are referenced to GND unless otherwise stated and labelled.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and V_{DD} = 5V environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply



3.2 Absolute Maximum Ratings

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Table 3-1 Absolute maximum ratings

Symbol	Description		Min.	Max.	Unit
T_A	Ambient temperature during operation		-40	85	°C
T_J	Junction temperature range		-40	105	°C
T_S	Ambient temperature during storage		-40	125	°C
V_{DD}	Voltage on external mains supply pin VDD		-0.3	6.0	V
V_{IN}	Voltage on I/O pins		-0.3	V_{DD}+0.3	V
$\|\triangle V_{DD_x}\|$	Voltage difference between each VDD of the main supply pins			20	mV
$\|\triangle V_{DDA}\|$	Voltage difference between V_{DD} and V_{DDA} of the main supply pins			200	mV
$\|\triangle GND_x\|$	Voltage difference between each GND of the common ground pins			20	mV
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (HBM) on common I/O pins		4K		V
I_{VDD}	Total combined current of all VDD main supply pins	CH643U		350	mA
		CH643L, CH643Q		550	

		CH643W		750	
I_{GND}	Total combined current on all GND common ground pins	CH643U		600	mA
		CH643L, CH643Q		1100	
		CH643W		1800	
I_{IO} (PA0-PA23)	PA sink current on any I/O pin			100	mA
	PA source current on any I/O pin			60	
I_{IO} (PB0-PB23)	PB sink current on any I/O pin			100	mA
	PB sink current on any I/O pin with duty cycle <= 1/8			400	
	PB source current on any I/O pin			30	
I_{IO} (PC0-PC20)	PC sink current on any I/O pin			40	mA
	PC source current on any I/O pin			30	
Pd	Maximum power consumption of the whole chip (also takes into account factors such as heat dissipation)	CH643U		700	mW
		CH643L, CH643Q		1000	
		CH643W		2000	
θ_{JA}	Package thermal resistance	CH643U	110		°C/W
		CH643L, CH643Q	80		
		CH643W	35		

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK} or F_{SYS}	Internal system bus frequency or microprocessor main frequency			48	MHz
V_{DD}	Operating supply voltage (nominal 5V)	Disable USB or PD function	2.0	5.5	V
		Enable USB or PD function	3.0	5.3	
V_{DDA}	Operating voltage of the analog section (without ADC)	V_{DDA} should be same as V_{DD}	2.0	5.5	V
	Operating voltage of the analog section (with ADC)		2.5	5.5	

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0.1	∞	us/V
	V_{DD} fall time rate		10	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Level selection of programmable voltage detector	PLS[1:0] = 00 (rising edge)		2.12		V
		PLS[1:0] = 00 (falling edge)		2.1		
		PLS[1:0] = 01 (rising edge)		2.32		V
		PLS[1:0] = 01 (falling edge)		2.3		
		PLS[1:0] = 10 (rising edge)		3.02		V
		PLS[1:0] = 10 (falling edge)		3		
		PLS[1:0] = 11 (rising edge)		4.02		V
		PLS[1:0] = 11 (falling edge)		4		
$V_{PVDhyst}$	PVD hysteresis			20		mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge		1.8		V
		Falling edge		1.78		V
$V_{PDRhyst}$	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		4	17	24	ms
	Other resets		6	9	20	us

Note: 1. Normal temperature test value.

3.3.3 Embedded Reference Voltage

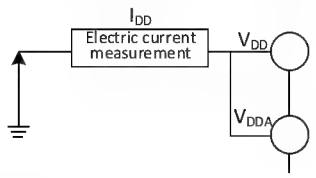
Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C~85°C	1.16	1.2	1.24	V
$T_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	Slow sampling recommended			11	$1/f_{ADC}$

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

When tested at room temperature VDD = 3.3V or 5V: all I/O ports configured with pull-up inputs, HSI = 48M. power consumption of all peripheral clocks enabled or disabled.

Table 3-6-1 Typical current consumption in Run mode, the data processing code runs from the internal Flash (VDD = 3.3V)

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(1)	Current in Run mode	Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	4.3	3.1	mA
			F_{HCLK} = 24MHz	3.3	2.7	
			F_{HCLK} = 8MHz	2.2	2.0	

Note: The above are measured parameters.

Table 3-6-2 Typical current consumption in Run mode, the data processing code runs from the internal Flash (VDD = 5V)

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(1)	Current in Run mode	Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	4.3	3.1	mA
			F_{HCLK} = 24MHz	3.3	2.7	
			F_{HCLK} = 8MHz	2.3	2.1	

Note: The above are measured parameters.

Table 3-7-1 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (VDD = 3.3V)

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(1)	Current in Sleep mode (In this case, peripheral power supply and clock are maintained)	Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	3.0	1.8	mA
			F_{HCLK} = 24MHz	2.1	1.5	
			F_{HCLK} = 8MHz	1.5	1.3	

Note: The above are measured parameters.

Table 3-7-2 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (VDD = 5V)

Symbol	Parameter	Condition	Typ.		Unit
			Enable all peripherals	Disable all peripherals	

I_{DD}(1)	Current in Sleep mode (In this case, peripheral power supply and clock are maintained)	Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	3.0	1.8	mA
			F_{HCLK} = 24MHz	2.1	1.5	
			F_{HCLK} = 8MHz	1.5	1.3	

Note: The above are measured parameters.

Table 3-8-1 Typical current consumption in Stop and Standby mode (VDD = 3.3V)

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}	Current in Stop mode	High-speed internal RC oscillator is off (no independent watchdog)	76	uA
	Current in Standby mode	Independent watchdog enabled	530	
		Independent watchdog disabled	58	

Note: The above are measured parameters.

Table 3-8-2 Typical current consumption in Stop and Standby mode (VDD = 5V)

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}	Current in Stop mode	High-speed internal RC oscillator is off (no independent watchdog)	90	uA
	Current in Standby mode	Independent watchdog enabled	550	
		Independent watchdog disabled	70	

Note: The above are measured parameters.

3.3.5 Internal Clock Source Characteristics

Table 3-9 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			48		MHz
$Duty_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	TA = 0°C~70°C	-2.0	±0.9	1.8	%
		TA = -40°C~85°C	-2.7	±1.2	2.4	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time		1.5		3.5	us
$I_{DD(HSI)}$	HSI oscillator power consumption			312		uA

3.3.6 Wakeup Time from Low-power Mode

Table 3-10 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	1	us
t_{wustop}	Wakeup from Stop mode	Wake up using HSI RC clock	10	us
$t_{WUSTDBY}$	Wakeup from Standby mode	Wake up using HSI RC clock	10	us

Note: The above are measured parameters.

3.3.7 Memory Characteristics

Table 3-11 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{prog}	Programming frequency(1)				48	MHz
t_{prog_page}	Page (256 bytes) programming time			1.5	2.0	ms
t_{erase_page}	Page (256 bytes) erase time			2.5	3.0	ms
t_{erase_sec}	Sector (1K bytes) erase time			2.7	3.3	ms

Note: 1. For the programming frequency of flash, read operation, program operation and erase operation are included. The clock is from HCLK.

Table 3-12 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25°C	100K			Times
t_{RET}	Data retention period		10			Years

3.3.8 I/O Port Characteristics

Table 3-13 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high-level voltage		(V_{DD}-2)* 0.36+1.3		V_{DD}	V
		V_{DD} = 5V	2.4		V_{DD}	V
		V_{DD} = 3.3V	1.8		V_{DD}	V
V_{IL}	Standard I/O pin, input low-level voltage		0		(V_{DD}-2)* 0.24+0.4	V
		V_{DD} = 5V	0		1.1	V
		V_{DD} = 3.3V	0		0.7	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis	V_{DD} = 5V	180	350		mV
I_{lkg}	Input leakage current		-2		2	uA
I_{PU}	Standard I/O pin weak pull-up current	V_{DD} = 5V	25	60	140	uA
		V_{DD} = 3.3V	12	30	65	uA
I_{PD}	PA0-PA15 pins weak pull-down current	V_{DD} = 5V	60	150	350	uA
		V_{DD} = 3.3V	30	75	180	uA
C_{IO}	Single I/O pin capacitor (without double I/O co-seal)			5		pF

Note: The above are guaranteed design parameters.

Output drive current characteristics

Table 3-14-1 Application 1: Full built-in mode LED dynamic drive. PWM output high, COM output low.

Symbol	Parameter	Condition: V_{DD} = 5V	Min.	Typ.	Max.	Unit
I_{SINK} COM IO	PB pin output low, pin dynamic sink current	Pin voltage = 1.7V		340		mA
		Pin voltage = 1V		270		
I_{SOURCE} PWM IO	PA pin output high, pin source current	Pin voltage = V_{DD} - 1V		21		mA
		Pin voltage = V_{DD} - 0.5V		18		

Table 3-14-2 Application 2: External PMOS method LED dynamic drive. PWM output low, COM control external PMOS output high.

Symbol	Parameter	Condition: V_{DD} = 5V	Min.	Typ.	Max.	Unit
I_{SINK} PWM IO	PA/PB pin output low, pin sink current	Pin voltage = 1.5V		38		mA
		Pin voltage = 0.5V		33		

Table 3-15 Output voltage characteristics Application: General purpose I/O

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL} (PA0-PA23)	Output low, pin sink current	I_{IO} = 100mA V_{DD} = 5V		0.4	V
V_{OH} (PA0-PA23)	Output high, pin source current	I_{IO} = 50mA V_{DD} = 5V	V_{DD}-0.4		V
V_{OL} (PA0-PA23)	Output low, pin sink current	I_{IO} = 60mA V_{DD} = 3.3V		0.4	V
V_{OH} (PA0-PA23)	Output high, pin source current	I_{IO} = 25mA V_{DD} = 3.3V	V_{DD}-0.4		V
V_{OL} (PB0-PB23)	Output low, pin sink current	I_{IO} = 100mA V_{DD} = 5V		0.4	V
V_{OH} (PB0-PB23)	Output high, pin source current	I_{IO} = 12mA V_{DD} = 5V	V_{DD}-0.4		V
V_{OL} (PB0-PB23)	Output low, pin sink current	I_{IO} = 60mA V_{DD} = 3.3V		0.4	V
V_{OH} (PB0-PB23)	Output high, pin source current	I_{IO} = 6mA V_{DD} = 3.3V	V_{DD}-0.4		V
V_{OL} (PC0-PC20)	Output low, pin sink current	I_{IO} = 15mA V_{DD} = 5V		0.4	V
V_{OH} (PC0-PC20)	Output high, pin source current	I_{IO} = 12mA V_{DD} = 5V	V_{DD}-0.4		V
V_{OL} (PC0-PC20)	Output low, pin sink current	I_{IO} = 8mA V_{DD} = 3.3V		0.4	V
V_{OH} (PC0-PC20)	Output high, pin source current	I_{IO} = 6mA V_{DD} = 3.3V	V_{DD}-0.4		V

Note: 1. The above are guaranteed design parameters.

2. If multiple IO pins are driven at the same time in the above conditions, the total current must not exceed the absolute maximum rating in section 3.2 of the table. Also when multiple IO pins are driven at the same time, the

current on the power/ground line is high and the resulting voltage drop causes the internal IO's to fall short of the supply voltage in the table, resulting in a drive current less than the nominal value.

Table 3-16 Input and output AC characteristics Application: General purpose IO

Pin	Symbol	Parameter	Condition	Min.	Max.	Unit
PA0-PA23	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD}=2.9~4.0V		30	MHz
			CL=50pF, V_{DD}=4.0~5.5V		40	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF, V_{DD}=2.9~4.0V		6	ns
			CL=50pF, V_{DD}=4.0~5.5V		5	ns
	$t_{r(IO)out}$	Output low to high rise time	CL=50pF, V_{DD}=2.9~4.0V		8	ns
			CL=50pF, V_{DD}=4.0~5.5V		6	ns
PB0-PB23	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD}=2.9~4.0V		15	MHz
			CL=50pF, V_{DD}=4.0~5.5V		20	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF, V_{DD}=2.9~4.0V		9	ns
			CL=50pF, V_{DD}=4.0~5.5V		7	ns
	$t_{r(IO)out}$	Output low to high rise time	CL=50pF, V_{DD}=2.9~4.0V		18	ns
			CL=50pF, V_{DD}=4.0~5.5V		15	ns
PC0-PC20	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD}=2.9~4.0V		30	MHz
			CL=50pF, V_{DD}=4.0~5.5V		40	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF, V_{DD}=2.9~4.0V		8	ns
			CL=50pF, V_{DD}=4.0~5.5V		7	ns
	$t_{r(IO)out}$	Output low to high rise time	CL=50pF, V_{DD}=2.9~4.0V		12	ns
			CL=50pF, V_{DD}=4.0~5.5V		10	ns

Note: The above are guaranteed design parameters.

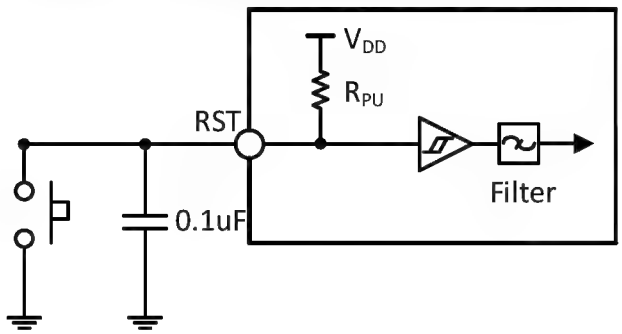
3.3.9 RST Pin Characteristics

Table 3-17 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{F(RST)}$	RST input pulse width		300			ns

Circuit reference design and requirements:

Figure 3-3 Typical circuit of external reset pin



3.3.10 USB PD Interface Characteristics

Table 3-18 PD interface characteristics, application: PD communication

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
tRise	Rising time	Time between 10% and 90% of the range, minimum value for no-load conditions.	300		600	ns
tFall	Falling time	Time between 10% and 90% of the range, minimum value for no-load conditions.	300		600	ns
vSwing	Output voltage swing (peak-to-peak)	Low voltage output mode, CL=50pF	1.04	1.12	1.20	V
Ipu	CC pull-up current	Pin voltage < V_{DD} - 1V, PUCC[1:0] = 11	64	80	96	uA
		Pin voltage < V_{DD} - 1V, PUCC[1:0] = 10	144	180	216	uA
		Pin voltage < V_{DD} - 1V, PUCC[1:0] = 01	264	330	396	uA

3.3.11 TIM Timer Characteristics

Table 3-19 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	MHz
R_{esTIM}	Timer resolution			16	位
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1363	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		1363	us

3.3.12 I2C Interface Characteristics

Figure 3-4 I2C bus timing diagram

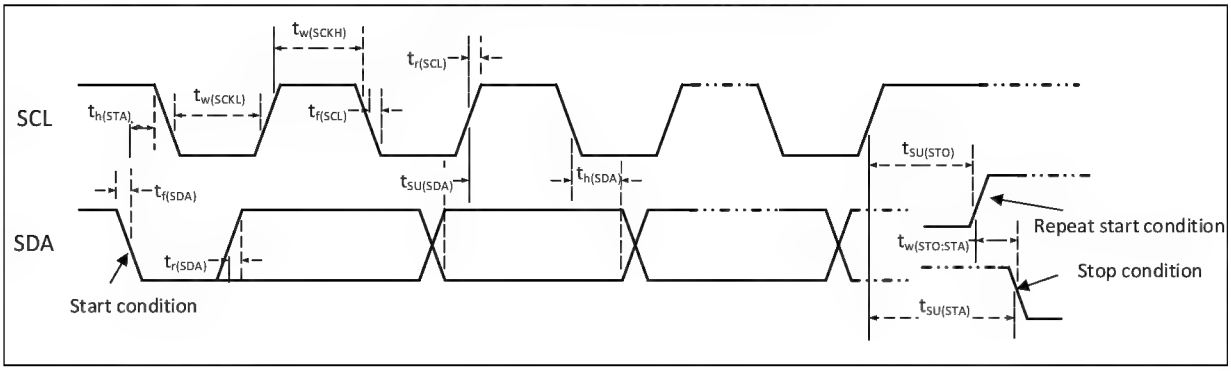


Table 3-20 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.13 SPI Interface Characteristics

Figure 3-5 SPI timing diagram in Master mode

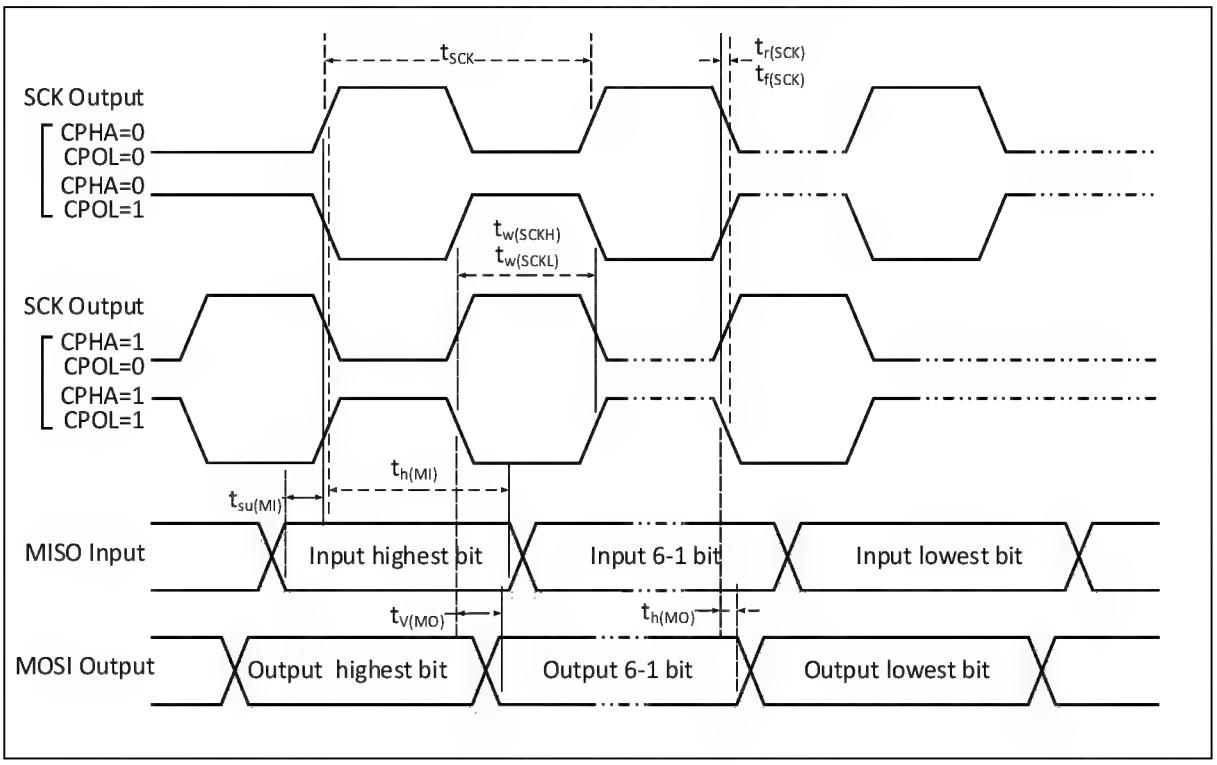


Figure 3-6 SPI timing diagram in Slave mode (CPHA=0)

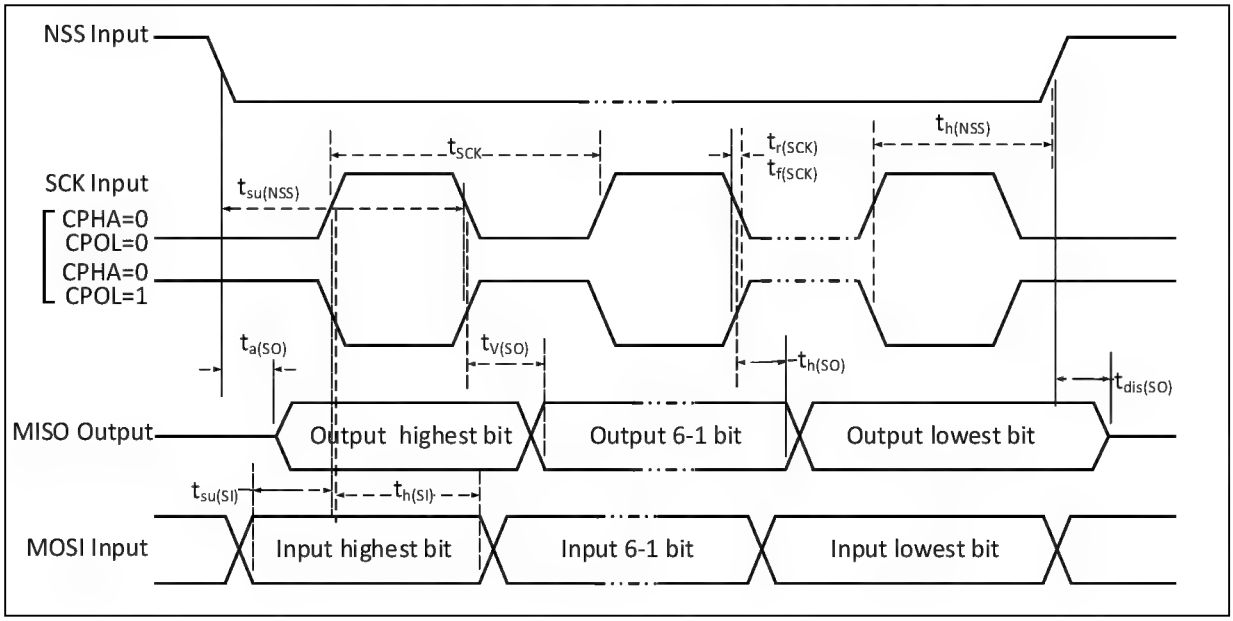


Figure 3-7 SPI timing diagram in Slave mode (CPHA=1)

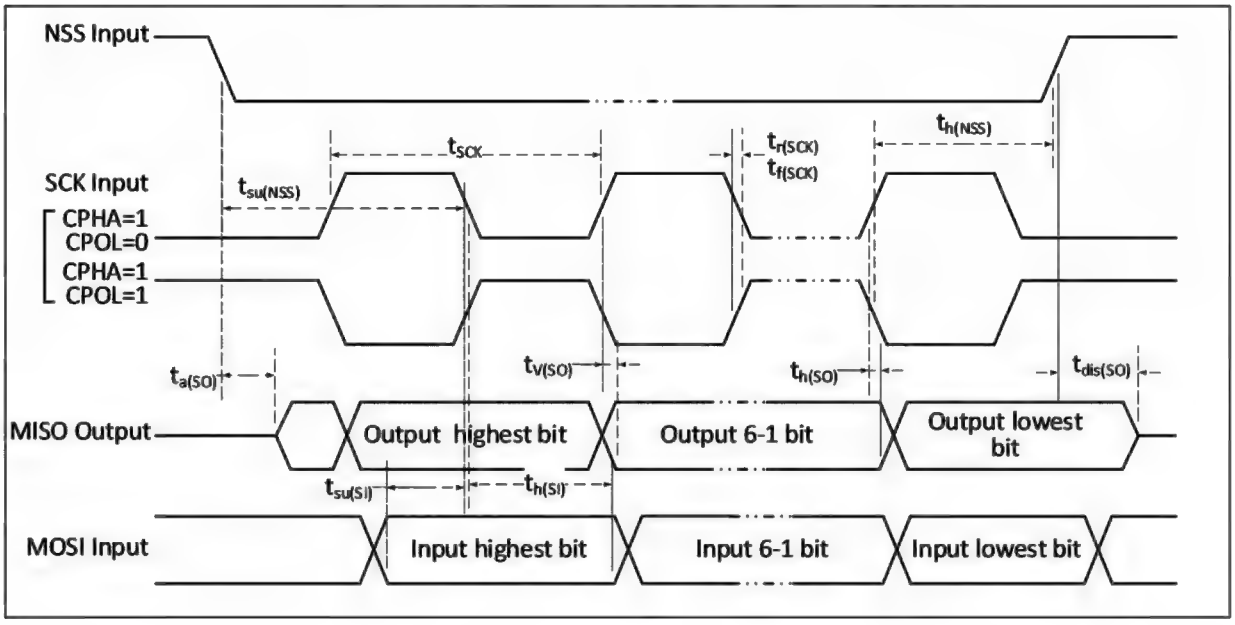


Table 3-21 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		24	MHz
		Slave mode		24	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high-level and low-level time	Master mode, f_{PCLK} = 24MHz, Prescaler factor = 4	70	100	ns

$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
$t_{SU(SI)}$		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
$t_{h(SI)}$		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$1t_{HCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)		25	ns
$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	15		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

3.3.14 USB Interface Characteristics

Table 3-22 USB interface I/O characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{DD}	USB operating voltage	Selection of USB parameters according to V_{DD} voltage	3.0	5.3	V
V_{SE}	Single-ended receiver threshold	Rated voltage	1.2	1.9	V
V_{OL}	Static output low level			0.3	V
V_{OH}	Static output high level		2.8		V

3.3.15 12-bit ADC Characteristics

Table 3-23 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	Rated performance	3.0	5	5.3	V
		Performance may be reduced	2.5		5.5	V
I_{DDA}	Supply current			290	480	uA
f_{ADC}	ADC clock frequency	V_{DD} >= 3.2V	3		8	MHz
		V_{DD} < 3.2V	3		6	MHz
f_S	Sampling rate	V_{DD} >= 3.2V	125		470	KHz
		V_{DD} < 3.2V	125		353	KHz
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_{ADC}	Sampling switch resistance		0.5	0.6	1.5	kΩ
C_{ADC}	Internal sample and hold capacitor			21		pF
t_{Iat}	Injected trigger conversion latency			1		$1/f_{ADC}$
t_{Iatr}	Regular trigger conversion latency			1		$1/f_{ADC}$
t_s	Sampling time			3.5		$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)		17		24	$1/f_{ADC}$

Note: The above are guaranteed design parameters.

Table 3-24 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EO	Offset error	f_{ADC} = 3 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 5V		±5		LSB
ED	Differential nonlinearity error			±2	±10	
EL	Integral nonlinearity error			±5	±20	

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-8 ADC typical connection diagram

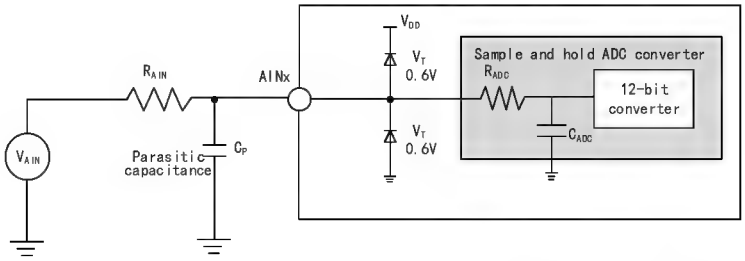
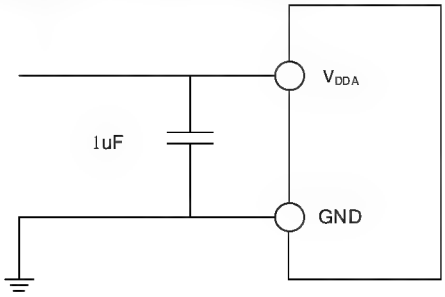


Figure 3-9 Analog power supply and decoupling circuit reference



3.3.16 OPA Characteristics

Table 3-25 OPA characteristics

Symbol	Parameter	Condition: V_{DD} = 5V	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	Recommended not less than 2.5V	2	5	5.5	V
C_{MIR}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage			3	9	mV
I_{LOAD}	Drive current	R_{LOAD} = 5kΩ			1	mA
I_{LOAD_PGA}	PGA mode drive current				400	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		210		uA
C_{MRR}(1)	Common mode rejection ratio	@1kHz		110		dB
P_{SRR}(1)	Power supply	@1kHz		70		dB

	rejection ratio					
A_V(1)	Open loop gain	C_{LOAD} = 5pF		110		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 5pF		13		MHz
P_M(1)	Phase margin	C_{LOAD} = 5pF		88		
S_R(1)	Slew rate limited	C_{LOAD} = 5pF		5		V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up, 0.1%	Input V_{DDA}/2, C_{LOAD} = 50pF, R_{LOAD} = 5kΩ			1	us
R_{LOAD}	Resistive load		5			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 5kΩ	V_{DDA}-300			mV
		R_{LOAD} = 20kΩ	V_{DDA}-50			
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 5kΩ			10	mV
		R_{LOAD} = 20kΩ			7	
PGA Gain(1)	NSEL=010b mode in phase	Gain =16, PA1=GND	-3		3	%
	Internal in-phase PGA	Gain = 4 V_{INP} < (V_{DDA}/7)	-1		1	%
		Gain = 8 V_{INP} < (V_{DDA}/15)	-1		1	%
		Gain = 16 V_{INP} < (V_{DDA}/31)	-1		1	%
		Gain = 32 V_{INP} <(V_{DDA}/63)	-1		1	%
Delta R	Absolute change in resistance		-15		15	%
EN(1)	Equivalent input voltage noise	R_{LOAD} = 5kΩ@1kHz		100		nV/ sqrt(Hz)
		R_{LOAD} = 20kΩ@1KHz		60		

Note: 1. The source simulation is not a real measurement.

2. The load current limits the saturated output voltage.

3.3.17 CMP Characteristics

Table 3-26 CMP voltage comparator characteristics

Symbol	Parameter	Condition: V_{DD} = 5V	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	Recommended not less than 2.5V	2	5	5.5	V
C_{MIR}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$(1)	Input offset voltage			4	12	mV
$I_{DDOPAMP}$	Current consumption			75		uA
t_D(1)	Comparator delay. V_{INP} varies from (V_{INN}-100mV) to (V_{INN}-100mV) change	0 ≤ VINN ≤ V_{DDA}		15	50	ns

V_{hys}(1)	Rated hysteresis voltage of the comparator	CMP_HYS = 0		0		mV
		CMP_HYS = 1		15		

Note: 1. Design parameters are guaranteed.

Chapter 4 Package and Ordering Information

Packages

Part No.	Package Form	Shaping Width	Pin Spacing	Package Description	Packing Type
CH643W	QFN80	9*9mm	0.4mm	Quad Flat No-Lead Package	Tray
CH643Q	LQFP64	7*7mm	0.4mm	Low Profile Quad Flat Pack	Tray
CH643L	LQFP48	7*7mm	0.5mm	Low Profile Quad Flat Pack	Tray
CH643U	QSOP28	3.9*9.9mm	0.635mm	Quarter-sized Outline Package	Tube

Note: 1. The packing type of QFP/QFN is usually tray.

*2. Size of tray: The size of Tray is generally a uniform size (322.6*135.9*7.62). There are differences in the size of the restriction holes for different package types, and there are differences between different packaging factories for tubes, please confirm with the manufacturer for details.*

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 4-1 QFN80 package

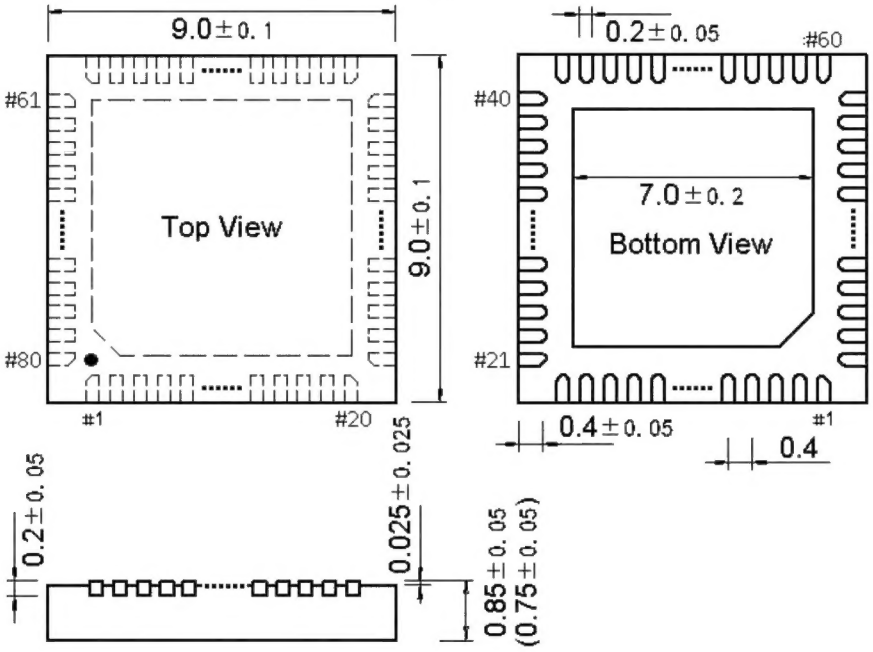


Figure 4-2 LQFP64 package

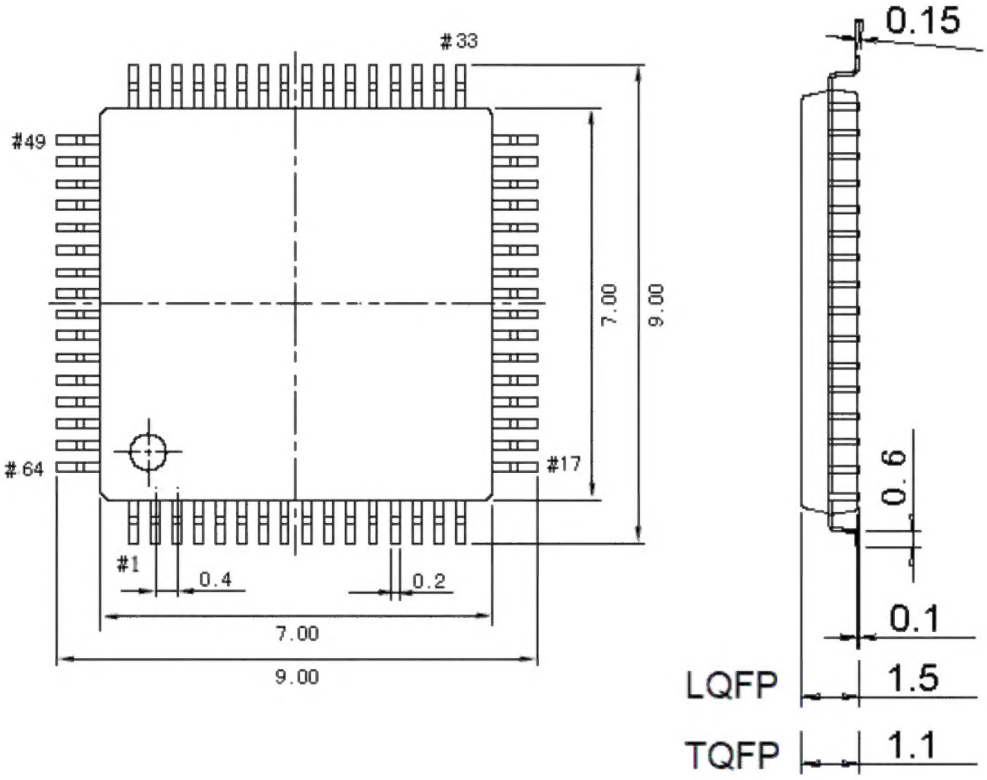


Figure 4-3 LQFP48 package

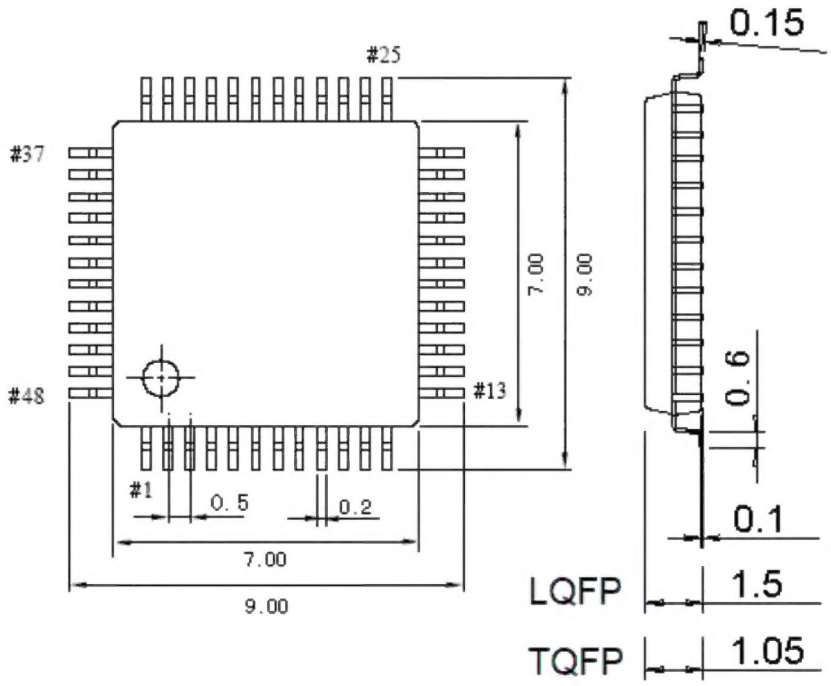
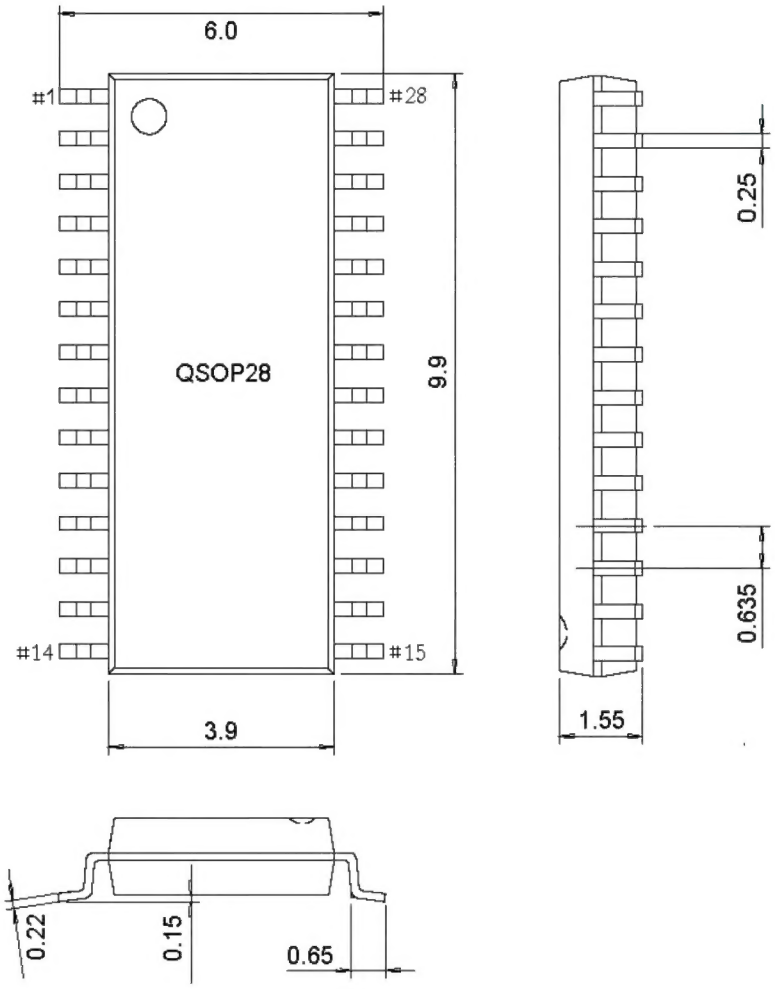



Figure 4-4 QSOP28 package